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UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

RICOH COMPANY, LTD.,

Plaintiff,

vs.

AEROFLEX INCORPORATED, AMI SEMICONDUCTOR, INC., MATROX ELECTRONIC SYSTEMS LTD., MATROX GRAPHICS INC., MATROX INTERNATIONAL CORP., MATROX TECH, INC., AND AEROFLEX COLORADO SPRINGS, INC.,

Defendants.

SYNOPSYS, INC.,

Plaintiff,

vs.

RICOH COMPANY, LTD.,

Defendant.

Case No. C03-4669 MJJ (EMC)

Case No. C03-2289 MJJ (EMC)

DECLARATION OF DENISE M. DE MORY IN SUPPORT OF MOTIONS FOR SUMMARY JUDGMENT

I, Denise M. De Mory, declare as follows:

1. I am a partner at the law firm of Howrey LLP, counsel for Aeroflex Incorporated, Aeroflex Colorado Springs, AMI Semiconductor, Inc., Matrox Electronic Systems, Ltd., Matrox Graphics Inc., Matrox International Corp., and Matrox Tech, Inc. and Synopsys, Inc. (collectively, the "Defendants") in this action. The following declaration is based on my personal knowledge. If called upon to testify, I could and would competently testify to the matters set forth below.

2. Attached as Exhibit 1 is a true and correct copy of United States Patent No. 4,922,432.

3. Attached as Exhibit 2 is a true and correct copy of Ricoh's Patent Final Contentions Pursuant to Patent L.R. 3-6 served March 24, 2006.

4. Attached as Exhibit 3 is a true and correct copy of Ricoh's Supplemental Patent Final Contentions Pursuant to Patent L.R. 3-6 served June 23, 2006. [FILED UNDER SEAL]

5. Attached as Exhibit 4 is a true and correct copy of Exhibit 65 to Ricoh's Supplemental Patent Final Contentions Pursuant to Patent L.R. 3-6 served June 23, 2006.

6. Attached as Exhibit 5 is a true and correct copy of Ricoh's Claim Construction Opening Brief served on August 27, 2004.

7. Attached as Exhibit 6 is a true and correct copy of Responsive Claim Construction Brief for U.S. Patent No. 4,922,432 (Re-Filed) served on September 14, 2004.

8. Attached as Exhibit 7 is a true and correct copy of Ricoh's Claim Construction Reply Brief served on September 20, 2004.

9. Attached as Exhibit 8 is a true and correct copy of April 7, 2005 Claim Construction Order.

10. Attached as Exhibit 9 are true and correct copies of Ricoh's Expert Report of Mario Papaefthymiou on Infringement by Aeroflex (Ex. 9A), AMI (Ex. 9B) and Matrox (Ex. 9C) served June 23, 2006. [FILED UNDER SEAL]

11. Attached as Exhibit 10 are true and correct copy of Expert Deposition of Mario Papeafthymiou dated August 11, 2006. [FILED UNDER SEAL]

12. Attached as Exhibit 11 are true and correct copies of Ricoh's Expert Report of Donald Soderman on Infringement by Aeroflex (Ex. 11A), AMI (Ex. 11B) and Matrox (Ex. 11C). [FILED UNDER SEAL]

13. Attached as Exhibit 12 are true and correct copy of Exhibit 1 to Ricoh's Expert Report of Donald Soderman on Infringement by Aeroflex, AMI and Matrox. [FILED UNDER SEAL]

14. Attached as Exhibit 13 are true and correct copy of Expert Deposition of Donald Soderman dated August 14 & 15, 2006. [FILED UNDER SEAL]

15. Attached as Exhibit 14 are true and correct copy of Ricoh's Supplemental Responses to ASIC Defendants' Requests for Admissions.

16. Attached as Exhibit 15 are true and correct copy of April 26, 1989 Amendment to Prosecution History for U.S. Patent No. 4,922,432.

17. Attached as Exhibit 16 are true and correct copy of November 24, 1989 Amendment to Prosecution History for U.S. Patent No. 4,922,432.

18. Attached as Exhibit 17 are true and correct copy of United States Patent No. 6,226,776.

19. Attached as Exhibit 18 are true and correct copy of Article titled "Implementing 'C' Designs in Hardware : A Full-Featured ANSI C to RTL Verilog Compiler in Action" by Donald Soderman.

20. Attached as Exhibit 19 are true and correct copy of Article titled "Implementing C Designs in Hardware: A Full-Featured ANSI C to RTL Verilog Compiler in Action" by Donald Soderman.

21. Attached as Exhibit 20 are true and correct copy of Article titled "Implementing C Alogrithms in Reconfigurable Hardware using C2Verilog" by Donald Soderman.

22. Attached as Exhibit 21 are true and correct copy of Book titled "Introduction to HDL-Based Design Using VHDL" by Steve Carlson bearing bates numbers 2SP 0768299-2SP 0768485.

23. Attached as Exhibit 22 are true and correct copy of United States Patent No. 4,703,435.

24. Attached as Exhibit 23 are true and correct copy of Deposition of Yoon-Pin Simon Foo dated May 31, 2006. [FILED UNDER SEAL]

25. Attached as Exhibit 24 are true and correct copy of master Thesis by Yoon-Pin Simon Foo titled "Managing VLSI D Design Data with A Relational Database System" bearing bates numbers FOO 000038-FOO 000156.

26. Attached as Exhibit 25 are true and correct copy of University of South Carolina Class Enrollment Sheet for Topics/Computer Engr bearing bates number SC 0003406.

27. Attached as Exhibit 26 are true and correct copy of Project Description for ECE890B Spring 1986 titled "A Knowledge-based Behavioral Description Translator" bearing bates number FOO 000189-FOO 000191 and Foo Deposition Exhibit No. 521.

28. Attached as Exhibit 27 are true and correct copy of Article titled "A Framework for Managing VLSI CAD Data" by Yoon-Pin Foo and H. Kobayashi bearing bates numbers KBSC000904-KBSC000913 and Foo Deposition Exhibit No. 509.

29. Attached as Exhibit 28 are true and correct copy of Article titled "A Knowledge Based System for VLSI Module Selection" by Yoon-Pin Foo and H. Kobayashi bearing bates numbers KBSC000904-KBSC000913 and Foo Deposition Exhibit No. 508.

30. Attached as Exhibit 29 are true and correct copy of Deposition Transcript of Hideaki Kobayashi dated May 25, 2006. [FILED UNDER SEAL]

31. Attached as Exhibit 30 are true and correct copy of document bearing bates numbers KBCS00009-KBSC00028. [FILED UNDER SEAL]

32. Attached as Exhibit 31 are true and correct copies of Translation of bates numbered page RCL0011957B. [FILED UNDER SEAL]

33. Attached as Exhibit 32 are true and correct copy of Translation of bates numbered page RCL0011958B. [FILED UNDER SEAL]

34. Attached as Exhibit 33 are true and correct copy of document bearing bates number RCL0011963. [FILED UNDER SEAL]

35. Attached as Exhibit 34 are true and correct copy of Exhibit A to the JCC Statement.

36. Attached as Exhibit 35 are true and correct copy of Master Thesis by Thaddeus J. Kowalski titled "The VLSI Design Automation Assistant: A Knowledge-Based Expert System".

37. Attached as Exhibit 36 are true and correct copy of Article titled "The VLSI Design Automation Assistant: From Algorithms to Silicon.

38. Attached as Exhibit 37 are true and correct copy of Deposition Transcript of Thaddeus J. Kowalski dated May 23, 2006. [FILED UNDER SEAL]

39. Attached as Exhibit 38 are true and correct copy of Request for Reexamination of United States Patent No. 4,922,432 to the United State Patent and Trademark Office dated January 17, 2006.

40. Attached as Exhibit 39 are true and correct copy of the United State Patent and Trademark Office Order Granting Reexamination of United States Patent No. 4,922,432 dated February 24, 2006

41. Attached as Exhibit 40 are true and correct copy of States Patent No. 4,922,432 File History.

42. Attached as Exhibit 41 are true and correct copy of document bates numbered RCL000064.

43. Attached as Exhibit 42 are true and correct copy of document bates numbered RCL000186.

44. Attached as Exhibit 43 are true and correct copy of Article titled "KBSC: A Knowledge Based Approach to Automatic Logic Synthesis" by H. Kobayashi.

45. Attached as Exhibit 44 are true and correct copy of document bates numbered KBSC000870-KBSC000872

46. Attached as Exhibit 45 are true and correct copy of 37 C.F.R. 1.56(a).

47. Attached as Exhibit 46 are true and correct copy of document bates numbered RCL00022.

48. Attached as Exhibit 47 are true and correct copy of document bates numbered RCL000188.

49. Attached as Exhibit 48 are true and correct copy of document bates numbered RCL000197.

50. Attached as Exhibit 49 are true and correct copy of 37 C.F.R. 1.97-1.99.

51. Attached as Exhibit 50 are true and correct copy of the corrected second supplemental Smith product declaration.

52. Attached as Exhibit 51 are true and correct copy of Deposition Transcript of Cliff Warren dated June 6, 2006. [FILED UNDER SEAL]

53. Attached as Exhibit 52 are true and correct copy of Deposition Transcript of David Tran, dated December 16, 2005 and June 6, 2006. [FILED UNDER SEAL]

54. Attached as Exhibit 53 are true and correct copy of Deposition Transcript of Reed Packer dated June 8, 2006. [FILED UNDER SEAL]

55. Attached as Exhibit 54 are true and correct copy of Expert Report of R. Fred Lipscomb. [FILED UNDER SEAL]

56. Attached as Exhibit 55 are true and correct copy of Expert Report of Maureen S. Loftus. [FILED UNDER SEAL]

57. Attached as Exhibit 56 are true and correct copy of Deposition Transcript of David Chiappini, Vol. 1 dated February 23, 2006. [FILED UNDER SEAL]

58. Attached as Exhibit 57 are true and correct copy of Deposition Transcript of David Chiappini, Vol. 3 dated June 7, 2006. [FILED UNDER SEAL]

59. Attached as Exhibit 58 are true and correct copy of Erik Olson Declaration in Support of Motion for Summary Judgment of Noninfringement under 35 U.S.C. Section 271(g).

60. Attached as Exhibit 59 are true and correct copy of Michael Heynes Declaration in Support of Motion for Summary Judgment of Noninfringement under 35 U.S.C. Section 271(g).

61 Attached as Exhibit 60 are true and correct copy of Second Supplemental Declaration of David Chiappini of Matrox Graphics, Inc.

62. Attached as Exhibit 61 are true and correct copy of Second Supplemental Declaration of Eric Boisvert of Matrox Electronic Systems.

63. Attached as Exhibit 62 are true and correct copy of document bearing bates numbers MGI0688426-MGI0688481. [FILED UNDER SEAL]

64. Attached as Exhibit 63 are true and correct copy of Schedule 2.1.1 the the Wagner Expert Report. [FILED UNDER SEAL]

65. Attached as Exhibit 64 are true and correct copy of Deposition Transcript of Eric Boivert dated June 6, 2006. [FILED UNDER SEAL]

66. Aeroflex performs ASIC design work for United States Government sub-contractors operating under a Government prime contract. Contracts executed for such work incorporate an authorization and consent clause (Federal Authorization Clause 52.227-1) either in the purchase order or contract between Aeroflex and the sub-contractor or in the U.S. Government prime contract under which the design work is performed. At least $4,804,851 of Aeroflex sales are pursuant to government contracts incorporating an express authorization and consent clause.

67. Aeroflex internally classifies its government contracts with a prefix of "gv" before the contract number. Some government prime contracts referenced on purchase orders for product sales pursuant to contracts designated "gv" for products at issue likely contain an authorization and consent clause. In some cases, the subcontractors are Sandia National Laboratory, Los Alamos National Laboratory, and Boeing Satellite Systems, for example. At least one prime contract was not locatable through a Freedom of Information Act request.

68. Attached as Exhibit 65 are true and correct copy of Complaint dated January 21, 2003.

69. Attached as Exhibit 66 are true and correct copy of document bearing bates numbers KBSC001109-KBSC001117.

70. Attached as Exhibit 67 are true and correct copy of translations of bates number 2SP0708285. [FILED UNDER SEAL]

71. Attached as Exhibit 68 are true and correct copy of Chart of Synopsys-Ricoh Contract.

72. Attached as Exhibit 69 are true and correct copy of document bearing bates numbers SP00001-00032. [FILED UNDER SEAL]

73. Attached as Exhibit 70 are true and correct copy of Verilog HDL Compiler Reference Manual bearing bates numbers SP04436-SP04536. [FILED UNDER SEAL]

74. Attached as Exhibit 71 are true and correct copy of Product of the Year Awards document bearing bates numbers SP04649-SP04651.

75. Attached as Exhibit 72 are true and correct copy of Synopsys ASIC Partnerships bearing bates numbers SP04707-SP04727. [FILED UNDER SEAL]

76. Attached as Exhibit 73 are true and correct copy of Article by Ann Steffora "Avant! Shakes Up Front-End Design" – Juniper CAE Software – Product Announcement, Electronic New, June 21, 1999

77. Attached as Exhibit 74 are true and correct copy of Article by Ray Weiss "Hot Design Comb", Electronic Engineering Times, May 14, 1990

78. Attached as Exhibit 75 are true and correct copy of Article "CAE Software Gould…, Electronic News, July 1, 1991".

79. Attached as Exhibit 76 are true and correct copy of document bearing bates numbers 2SP0763439-2SP763460.

80. Attached as Exhibit 77 are true and correct copy of AMIS website print out.

81. Attached as Exhibit 78 are true and correct copy of AMIS website print out.

82. Attached as Exhibit 79 are true and correct copy of UTMC website print out.

83. Attached as Exhibit 80 are true and correct copy of Synopsys web site print out.

84. Attached as Exhibit 81 are true and correct copy of Synopsys web site print out.

85. Attached as Exhibit 82 are true and correct copy of Ricoh's Amended Complaint

86. Attached as Exhibit 83 are true and correct copy of document bearing bates number MGI0033893-MGI0033908. [FILED UNDER SEAL]

87. Attached as Exhibit 84 are true and correct copy document bearing bates number RCL011421-RCL011422. [FILED UNDER SEAL]

88. Attached as Exhibit 85 are true and correct copy document bates numbered SP0168741-SP0168776. [FILED UNDER SEAL]

89. Attached as Exhibit 86 are true and correct copy document bates numbered SP0167847-SP0167881. [FILED UNDER SEAL]

90. Attached as Exhibit 87 are true and correct copy document bates numbered SP0121654-SP0121667. [FILED UNDER SEAL]

91. Attached as Exhibit 88 are true and correct copy document bates numbered MGI0001490. [FILED UNDER SEAL]

92. Attached as Exhibit 89 are true and correct copy Deposition Transcript of Shir-Shen Chang dated January 5, 2006. [FILED UNDER SEAL]

93. Attached as Exhibit 90 are true and correct copy Deposition Transcript of Karen L. Pieper dated December 12, 2005. [FILED UNDER SEAL]

Executed this 18th day of August, 2006, at San Francisco, California.

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct.

Denise M. De Mory

EXHIBIT 59

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UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

RICOH COMPANY, LTD.,

Plaintiff,

vs.

AEROFLEX INCORPORATED, et al.,

Defendants.

SYNOPSYS, INC.,

Plaintiff,

vs.

RICOH COMPANY, LTD.,

Defendant.

Case No. C03-04669 MJJ (EMC)

Case No. C03-2289 MJJ (EMC)

DECLARATION OF MICHAEL HEYNES IN SUPPORT OF DEFENDANTS' NOTICE OF MOTION AND MOTION FOR SUMMARY JUDGMENT OF NONINFRINGEMENT UNDER 35 U.S.C. §271(g)

Date: August 9, 2005
Time: 9:30 a.m.
Courtroom: 11, 19th Floor
Judge: Martin J. Jenkins

I, Michael Heynes, declare as follows:

1. I am a senior engineer with nearly forty years of experience developing and managing silicon chip fabrication technology. I was a principal contributor of technical content to the 2005 book "Demystifying Chipmaking." I have done consulting work and training on fabrication for numerous companies, including Applied Materials, Lam Research, Texas Instruments, and Motorola. I have been involved in the fabrication of at least one hundred different chips. I have a Ph.D. in Physical Chemistry from London University, where I wrote my thesis on Molecular Structure and Dielectric Properties of Silicates. I am a member of the Electrochemical Society and Institute of Electrical and Electronic Engineers (IEEE). My CV is attached hereto as Exhibit A. I make this Declaration of my personal knowledge, and if called as a witness, I could and would testify competently to the statements contained herein.

2. In forming the opinions set forth at the end of this declaration, I have considered and reviewed the text of United States Patent No. 4,922,432 ("the '432 patent").

3. ASIC design and chip manufacturing are separate phases. Very often these phases include separate companies, or at the very least, different departments within a company.

4. ASIC design culminates in the "tape out" of mask data. The mask data can then be used in photomask generation. The photomasks are subsequently used in ASIC manufacture. A chip is manufactured in layers; the overall layout is partitioned appropriately by the design software. Each layer is a pattern that must be reproduced on the wafer. These patterned layers, when stacked up, become the electronic components of the chip, all wired together. The individual layer patterns are transferred to the chip using a photolithographic technique. A template, called a photomask, is made for each layer.

5. Photomask manufacture includes the high level steps of:

i) photomask generation;
ii) prototype chip verification; and
iii) qualification for transfer to ASIC manufacturing.

6. Photomask generation includes many steps. These steps include, for each layer:

i) The mask-making company receives a computer file containing the design for each photomask.
ii) A blank, chrome-coated or other type of film-coated quartz glass plate is covered with photoresist or electron beam resist (photo-sensitive polymer or plastic sensitive to light or electron beams, respectively).
iii) Then the plate is processed in a computer-controlled electron beam (e-beam) tool or a laser pattern generator that exposes the desired pattern in the resist through multiple exposure steps. The mask data is used to produce the instructions for the machine that creates the pattern in the resist.
iv) Developer solution removes the unwanted resist, creating the desired pattern, and the pattern is inspected.
v) The remaining resist serves as the template (resist mask) for a wet etching process to remove the chrome not protected by the resist pattern.
vi) When the etching is completed, the resist mask is stripped off.
vii) The photomask receives a final inspection, and any defects are repaired.

7. The end result of the photomask generation steps is the creation of the desired pattern in the chrome or other layer on the glass surface, which can then be used as a mask. Typically, for state of the art chips, at least 25 to 30 masks are required to manufacture one chip design. Once the prototype photomasks have been finalized, the hundreds of steps necessary for actually manufacturing the integrated circuit can proceed using those photomasks.

8. After the prototype photomasks are generated, there is a prototype chip verification. This verification includes:

i) Running a small number of wafers using the new prototype photomasks;
ii) Electrically testing chips, in wafer form;
iii) Assembling and packaging chips; and
iv) Electrically testing packaged chips.

9. Once prototype chip verification is complete, the qualification for transfer to ASIC manufacturing occurs. Qualification includes up to thousands of computer-controlled electrical tests to characterize the product in terms of performance. Qualification can also include reliability testing, such as burn-in and temperature/humidity tests.

10. After the prototype chip verification and qualification are successfully completed, the photomasks are considered to be finalized.

11. The high level steps of ASIC manufacture include:

i) wafer fabrication; and
ii) assembly and test.

12. ASIC manufacture begins with wafer fabrication. Typically, many hundreds of ASIC chips are formed on a single wafer. Wafer fabrication minimally involves many hundreds of individual steps. These steps can be broken down and fall into two categories, the front end of the line (FEOL) and the back end of the line (BEOL). In the FEOL, the transistors and other devices are formed in and on the wafer surface. In the BEOL, the devices are wired together with metallization processes and the circuit is protected with a final sealing layer. These manufacturing steps typically include, but are not limited to, processes such as chemical vapor deposition, physical vapor deposition, etching, and chemical mechanical polishing.

13. After wafer fabrication, the circuits on the wafer are complete, but still in wafer form and have not yet been tested. During wafer sort, each chip is electrically tested for functionality. Once the functional chips are identified, packaging begins. The industry also refers to this phase of chip manufacture as assembly and test (A/T). During this phase, the wafers are separated, or diced, into individual chips, and the functional chips are placed into protective packages. Packaging typically takes place in a separate department of the semiconductor producer or often in a foreign plant. After packaging, there are further electrical tests, which are even more extensive than the electrical tests carried out at the wafer level.

14. The wafer fabrication processes fall into four basic operations. They are layering, patterning, doping, and heat treatments. These processes are used repeatedly in the wafer fabrication process. The exact sequence is determined by the "construction" of the transistor used along with other physical attributes of the circuit components, and the interconnection wiring of the circuits.

i) Layering (otherwise known as thin film formation): Layers used in the circuit as dielectrics, conductors, or semiconductors are grown or deposited on the wafer surface. Ways of forming layers or films include chemical vapor deposition, physical vapor deposition, and oxidation.

ii) Patterning: The electrical functioning of an IC is dependent on the physical dimensions of the components formed in and on the wafer surface and the electrical characteristics (such as electrical carrier concentrations, and the electrical resistance at the wafer surface). The vertical dimensions (d) are created by the thickness of the layers and by the depth of the doped regions.

The horizontal dimensions (w and l) are created during the patterning process. This process uses a mask, as described above, which has the required horizontal dimensions and the relative position of the components set in chrome on a glass

plate. The mask is used as a stencil to transfer the mask dimensions into a layer of a photoresist. The resultant image in the photoresist is generally transferred into the wafer surface through an etching process.

The steps in patterning include:

1. Baking wafers and priming surfaces.
2. Coating wafers with photoresist, known as spinning.
3. Softbaking to evaporate solvents.
4. Aligning and exposing pattern in photoresist.
5. Developing resist to remove exposed photoresist.
6. Hardbaking to harden the photoresist.
7. Inspecting for defects, contamination, measuring pattern dimensions, pattern distortions, etc.
8. Etching to remove unwanted material through openings in the photoresist.
9. Removing photoresist.
10. Final inspection for defects, contamination, measure pattern dimensions, pattern distortions, etc.

iii) Doping: Electrically active chemical elements are put into the wafer surface to modify the electrical properties of the silicon through ion implantation or diffusion techniques.

iv) Heat Treatments: Many thermal processes are involved throughout the wafer fabrication cycle for many different purposes, such as low temperature steps to evaporate solvents from the photoresist, and high temperature steps to grow thin oxide films on the silicon.

15. The conclusion of the wafer fabrication process is the wafer sort to identify the functioning chips.

16. After the wafers are fabricated and sorted, assembly and test occurs. Assembly and test includes several steps, including:

i) Wafer Backside Preparation: To thin the wafer in preparation for packaging.
ii) Die Separation: To cut individual chips from the wafer.
iii) Die Pick: To select functioning die and place them in package.
iv) Die Attach: To attach the die to the package.
v) Wire Bonding: To connect leads between die and package.
vi) Pre Seal Inspection: To inspect wire bonding.
vii) Seal: To encapsulate the die in the package.
viii) Marking: To identify product.
ix) Final Electrical and Environmental Tests: To test that chips fully meet customer specifications.

17. After the chips finish the assembly and test process, they are packed and shipped to the customer.

18. Based on claims 13-17 and the '432 patent's description, it is my opinion that claim 13-17's processes are not directed to manufacture at all, rather they are completely directed toward design. Therefore, Claim 13-17's processes are not processes for "directly manufacturing" ASIC chips.

19. While the design information, particularly the mask data, is used in the manufacture of photomasks, it is not used directly in the manufacture of ASIC chips. None of these steps following the "tape out" is part of the patented process of the '432 Patent.

20. As described above, the mask data is subsequently used in other processes to produce masks, not ASIC chips. The claimed processes for generating netlists and mask data are not even steps in the manufacture of masks, let alone ASIC chips. There are many manufacturing steps that lie between the end product of the processes of the '432 patent and masks, and many hundreds of additional manufacturing steps that lie between the masks and the manufactured ASIC chips.

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct. This declaration was executed in San Mateo, California on June 14, 2005.

Dr. Michael Heynes

EXHIBIT A

Michael S. Heynes

1501 W. Hillsdale Blvd., #111, San Mateo, CA 94402
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Overview
Senior engineer with broad semiconductor industry experience managing silicon chip fabrication technology, primarily in CMOS.
Managed engineering groups responsible for new product and new process module development, in both MOS and bipolar technologies.
Managed technology transfer and bring-up of new manufacturing equipment and facilities.
Much work in training in recent years.

Work Experience

Consultant **7/98 to date**
Primarily engaged in technical training
- Generated and taught classes on a wide range of semiconductor industry topics.
- Wrote and reviewed scripts for training videos.
  Reviewed and advised on drafts for technical publications and product marketing brochures (in association with Semiconductor Services).

Lam Research Corp., Fremont, CA **95 –98**
Senior instructor
Developed and presented classes on a range of semiconductor topics with emphasis on applications of Lam equipment in chip manufacturing.

Teledyne Components, Mountain View, CA **90-95**
Senior Staff Scientist
Developed and transferred to manufacturing CMOS and bipolar process technology for digital and analog circuit applications.
Carried out a study to evaluate difficulties and market potential for micro-machined sensors (MEMS)

Previous positions

- Senior Member Technical Staff, Gain Electronics (Somerville, NJ)
  A Bell Laboratories spin-off formed to produce digital gallium arsenide chips.
- Manager, CMOS Technology Development, American Microsystems (Santa Clara and Pocatello, Idaho)
  Included two year assignment to acquire and bring up new equipment and transfer CMOS manufacturing technology to a new joint-venture operation with a major company in Austria.

- Manager, IC Pilot Line, Microtechnology, (A Sunnyvale CMOS start-up, later acquired by Storage Technology.)
  Responsible for running new chip design prototypes.
- Director, Process Technology Development, Nortec Electronics, an early MOS start-up in Santa Clara.
  Developed a range of MOS technology processes.

- Early work at Signetics(Philips), Raytheon, Shockley Transistor included silicon crystal and epitaxial film growth, chemical vapor deposition (CVD), oxidation, diffusion, development of bipolar RF/ microwave power transistors.

Education
B.Sc., Chemistry, Birmingham University, England
Ph.D., Physical Chemistry, London University, England
(Molecular Structure and Dielectric Properties of Silicates)

Principal contributor of technical content to book : "Demystifying Chipmaking"
Yanda, Heynes, Miller. (Elsevier 2005; ISBN 0-7506-7760-0)

Member, Electrochemical Society and IEEE (Institute of Electrical and Electronic Engineers)

EXHIBIT 60

Teresa M. Corbin (SBN 132360)
Denise M. De Mory (SBN 168076)
Jaclyn C. Fink (SBN 217913)
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Attorneys for Plaintiff SYNOPSYS, INC.
and for Defendants AEROFLEX INCORPORATED, AMI SEMICONDUCTOR, INC., MATROX ELECTRONIC SYSTEMS, LTD., MATROX GRAPHICS, INC., MATROX INTERNATIONAL CORP., MATROX TECH, INC., and AEROFLEX COLORADO SPRINGS, INC.

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

RICOH COMPANY, LTD., Plaintiff, vs. AEROFLEX INCORPORATED, AMI SEMICONDUCTOR, INC., MATROX ELECTRONIC SYSTEMS LTD., MATROX GRAPHICS INC., MATROX INTERNATIONAL CORP., MATROX TECH, INC., AND AEROFLEX COLORADO SPRINGS, INC. Defendants.	Case No. C03-04669 MJJ (EMC) Case No. C03-2289 MJJ (EMC) **SECOND SUPPLEMENTAL PRODUCT DECLARATION OF DAVID CHIAPPINI OF MATROX GRAPHICS**
SYNOPSYS, INC., Plaintiff, vs. RICOH COMPANY, LTD., Defendant.	

I, David Chiappini, declare as follows:

1. I am the ASIC Project Director of Matrox Graphics Inc. ("Matrox Graphics"). I have been an employee of Graphics since June 1996, and I am familiar with our operations and facilities from February 1997 to the present. I make this Declaration of my personal knowledge, and if called as a witness, I could and would testify competently to the statements contained herein.

2. Engineers at Matrox Graphics design application specific integrated circuits (ASICs). In designing ASICs, our engineers use various types of libraries in association with the Design Compiler® software from Synopsys.

3. We have used the following "Commercial ASICs" (using the specified technology libraries as defined in the May 5, 2006 Amended Stipulation Re Supplemental Production In Accordance With Judge Chen's April 20, 2006 Order and Order Thereon (Ex. A):

#	PRODUCT	DESCRIPTION	LIBRARY	SYNTHESIZED IN US
1	Cyclone	Graphics processing unit	NEC 0.5um	No
2	Eclipse	Graphics processing unit	NEC 0.35um	No
3	EclipsePCI	Graphics processing unit	NEC 0.35um	No
4	Calao	Graphics processing unit	NEC 0.25um	No
5	Toucan	Graphics processing unit	NEC 0.25um	No
6	Condor	Graphics processing unit	UMC 0.18um	No
7	Condor Plus	Graphics processing unit	UMC 0.18um	No
8	Parhelia	Graphics processing unit	UMC 0.15um	Yes
9	Sundog	Graphics processing unit	UMC 0.15um	Yes
10	Parhelia8x	Graphics processing unit	UMC 0.15um	Yes
11	Sunex	Graphics processing unit	UMC 0.15um	No
12	Maven	Video co-processing unit	NEC 0.25um	Synthesized by party not in suit located outside the US

4. The following product included on the original Declaration has been removed from the list above because, after further investigation, it was determined that it was synthesized prior to the damages period:

#	PRODUCT	DESCRIPTION	LIBRARY	REASON FOR REMOVAL
1	Mistral	Graphics processing unit	NEC 0.35um	Synthesized prior to damages period

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct. This declaration was executed in Dorval, Quebec on May 9, 2006.

David Chiappini

EXHIBIT A

Teresa M. Corbin (SBN 132360)
Denise M. De Mory (SBN 168076)
Jaclyn C. Fink (SBN 217913)
HOWREY LLP
525 Market Street, Suite 3600
San Francisco, California 94105
Telephone: (415) 848-4900
Facsimile: (415) 848-4999

Attorneys for Defendants AEROFLEX INCORPORATED, AEROFLEX COLORADO SPRINGS, INC., AMI SEMICONDUCTOR, INC., MATROX ELECTRONIC SYSTEMS, LTD., MATROX GRAPHICS, INC., MATROX INTERNATIONAL CORP., and MATROX TECH, INC.

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

RICOH COMPANY, LTD., Plaintiff, vs. AEROFLEX INCORPORATED, AMI SEMICONDUCTOR, INC., MATROX ELECTRONIC SYSTEMS LTD., MATROX GRAPHICS INC., MATROX INTERNATIONAL CORP., MATROX TECH, INC., AND AEROFLEX COLORADO SPRINGS, INC., Defendants.	Case No. C03-04669 MJJ (EMC) **AMENDED STIPULATION AND ORDER RE SUPPLEMENTAL PRODUCTION IN ACCORDANCE WITH JUDGE CHEN'S APRIL 20, 2006 ORDER** ; ORDER THEREON

IT IS HEREBY STIPULATED AND AGREED by and between Ricoh Company, Ltd. ("Ricoh") and Aeroflex Incorporated, AMI Semiconductor, Inc., Matrox Electronics Systems, Ltd., Matrox Graphics Inc., Matrox International Corp., Matrox Tech., Inc. and Aeroflex Colorado Springs, Inc. (the "Defendants") that:

1. A "Commercial ASIC" is any ASIC (as defined in U.S. Patent No. 4,922,432 at Col. 1:13-17) that was, between 1997 and the present, (1) synthesized using Design Compiler for which (2) revenue was received and (3) one or more physical ASICs were manufactured (whether considered to

be a prototype or not). To avoid any doubt, all three criteria must be met and all three criteria must have occurred between 1997 and the present for an ASIC to qualify as a "Commercial ASIC."

2. Subject to the limitations set forth in the paragraphs below, the Defendants will identify and produce documents relating to Commercial ASICs synthesized between 1997 and the present by subsidiaries, including those ASICs for which synthesis was performed before acquisition of the subsidiary or its assets, for any Commercial ASIC either synthesized in the United States or sold in the United States, except that Commercial ASICs synthesized before an acquisition or asset purchase will not be identified if the acquiring party did not obtain rights to the ASICs. The Defendants will identify and produce documents, subject to the limitations set forth below, relating to Commercial ASICs synthesized by third parties provided that the synthesis was done at the request, direction or control of any named party.

3. For all newly identified products, Ricoh agrees to accept production of only "product packages" and financial information. The "product package" for a newly identified Commercial ASIC will include, to the extent it exists and is within the producing Defendant's possession, custody or control, the (1) script(s), including DC setup files, (2) inputs, including RTL inputs,[1] (3) technology library(ies), (4) log file(s) and (5) netlist(s) for the newly identified Commercial ASIC.

4. For all newly identified Commercial ASICs, the Defendants agree to produce financial documents including sales and cost information to the extent such information exists and is within the producing Defendant's possession, custody or control, with the following qualification: if all synthesis was done in the United States, or the RTL or technology library was supplied from the United States, or the netlist or mask data was shipped into the United States for manufacturing, then the producing Defendant will produce worldwide sales information for the newly identified Commercial ASIC. Otherwise, the producing Defendant will produce only information regarding sales in the United States.

---

[1] The Defendants shall determine whether any third party, non-Synopsys software (e.g., a flowchart translator) was used to convert an input specification to RTL. If so, the Defendants shall identify such third party software and produce the input specification and the converted RTL.

5. The Defendants will update their product declarations and library declarations (to the extent such updates are called for by newly identified ASICs) by May 10.

6. The Defendants will make good faith efforts to produce all documents by May 15. The product packages will be produced in an electronically searchable format. The financial documents will be produced in bates labeled and a native electronic format, to the extent such format exists.

7. To the extent that a particular Defendant does not have a complete product package or financial information for a newly identified ASIC, the Defendant will inform Ricoh that it does not have such information. To the extent the Defendant knows if such information is in the possession, custody, and control of a third party, it will identify such third party. To the extent that responsive information is the possession, custody or control of third parties known to the Defendants, the Defendants will cooperate in good faith in assisting Ricoh to obtain such information by requesting that the third party provide such information to it. Ricoh, however, understands that the Defendants' obligations under this Stipulation are limited to making good faith requests.

8. The Defendants will make good faith efforts to provide additional 30(b)(6) deponents before June 9. The Defendants will work in good faith to try to schedule depositions such that all or most of the 30(b)(6) deponents are produced in one location in a one week period.

9. This Stipulation resolves the issues raised by Ricoh's Motion for Sanctions filed on February 21, 2006. If the Defendants fail to perform in accordance with any of the terms of this Stipulation, Ricoh reserves the right to seek evidentiary, monetary, or other sanctions.

10. To the extent that new Commercial ASICs are identified, Ricoh and the Defendants agree that Ricoh's Final Infringement Contentions served on March 24, 2006 shall, in substantial part, satisfy Ricoh's obligations to produce Final Infringement Contentions with regard to the newly identified Commercial ASICs. Ricoh, however, shall supplement its Final Infringement Contentions for each newly identified Commercial ASIC by identifying only the inputs that satisfy the following elements of claim 13: "storing data describing a set of available integrated circuit hardware cells for performing the actions and conditions defined in the stored set" and "describing for a proposed application specific integrated circuit a series of architecture independent actions and conditions." To the extent that the Defendants produced declarations, documents, and deponents as set forth above,

Ricoh will provide this supplement on or before June 19, 2006. In the event that the above deadlines are not met, the parties will meet and confer in good faith regarding an appropriate time for supplementation.

Dated: May 5, 2006

HOWREY LLP

By: /s/ Denise M. De Mory
Attorneys for Defendants AEROFLEX INCORPORATED, AEROFLEX COLORADO SPRINGS, INC., AMI SEMICONDUCTOR, INC., MATROX ELECTRONIC SYSTEMS, LTD., MATROX GRAPHICS INC., MATROX INTERNATIONAL CORP. and MATROX TECH, INC.

Dated: May 5, 2006

DICKSTEIN SHAPIRO MORIN & OSHINSKY, LLP

By: /s/Kenneth W. Brothers
Kenneth W. Brothers (*pro hac vice*)

ALTSHULER, BERZON NUSSBAUM, RUBIN & DEMAIN
Jeffrey B. Demain
Attorneys for Plaintiff and Defendant RICOH COMPANY, LTD.

ORDER

Pursuant to stipulation, it is so ordered. ~~The continued hearing on Ricoh's Motion for Sanctions set for May 3, 2006 is hereby vacated.~~

This order ~~terminates Docket No. 358.~~ modifies the Order entered as Docket No. 448.

DATED: May 8, 2006

UNITED STATES DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA
IT IS SO ORDERED
AS MODIFIED
Judge Edward M. Chen

PROOF OF SERVICE

STATE OF CALIFORNIA)
) ss.:
COUNTY OF SAN FRANCISCO)

I am employed in the County of San Francisco, State of California. I am over the age of 18 and not a party to the within action. My business address is 525 Market Street, Suite 3600, San Francisco, California 94105.

On May 10, 2006 I served on the interested parties in said action the within:

SECOND SUPPLEMENTAL PRODUCT DECLARATION OF DAVID CHIAPPINI OF MATROX GRAPHICS

by causing said document to be sent by Electronic Mail on May 10, 2006 to the email addresses indicated for the parties listed below and by placing a true copy thereof in a sealed envelope(s) addressed as stated below and causing such envelope(s) to be delivered as follows:

Gary M. Hoffman, Esq.
HoffmanG@dsmo.com
Dickstein Shapiro Morin & Oshinsky, LLP
2101 L Street, N.W.
Washington, DC 20037-1526

Facsimile No.: (202) 887-0689

Jeffrey Demain, Esq.
jdemain@altshulerberzon.com
Altshuler, Berzon, Nussbaum, Rubin & Demain
177 Post Street, Suite 300
San Francisco, CA 94108

Facsimile No.: (415) 362-8064

Edward A. Meilman, Esq.
MeilmanE@dsmo.com
Dickstein Shapiro Morin & Oshinsky, LLP
1177 Avenue of the Americas
New York, NY 10036-2714

Facsimile No.: (212) 896-5471

☒ (OVERNIGHT DELIVERY) on May 10, 2006 by depositing in a box or other facility regularly maintained by Federal Express, an express service carrier, or delivering to a courier or driver authorized by said express service carrier to receive documents, a true copy of the foregoing document in sealed envelopes or packages designated by the express service carrier, addressed as stated above, with fees for overnight delivery paid or provided for and causing such envelope(s) to be delivered by said express service carrier on.

I declare under penalty of perjury that I am employed in the office of a member of the bar of this Court at whose direction the service was made and that the foregoing is true and correct.

Executed on May 10, 2006, at San Francisco, California.

Peter L. Kasenenko
(Type or print name)

Peter L. Kasenenko
(Signature)

EXHIBIT 61

Teresa M. Corbin (SBN 132360)
Denise M. De Mory (SBN 168076)
Jaclyn C. Fink (SBN 217913)
HOWREY LLP
525 Market Street, Suite 3600
San Francisco, California 94105
Telephone: (415) 848-4900
Facsimile: (415) 848-4999

Attorneys for Plaintiff SYNOPSYS, INC. and for Defendants AEROFLEX INCORPORATED, AMI SEMICONDUCTOR, INC., MATROX ELECTRONIC SYSTEMS, LTD., MATROX GRAPHICS, INC., MATROX INTERNATIONAL CORP., MATROX TECH, INC., and AEROFLEX COLORADO SPRINGS, INC.

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

RICOH COMPANY, LTD., Plaintiff, vs. AEROFLEX INCORPORATED, AMI SEMICONDUCTOR, INC., MATROX ELECTRONIC SYSTEMS LTD., MATROX GRAPHICS INC., MATROX INTERNATIONAL CORP., MATROX TECH, INC., AND AEROFLEX COLORADO SPRINGS, INC. Defendants.	Case No. C03-04669 MJJ (EMC) Case No. C03-2289 MJJ (EMC) **SECOND SUPPLEMENTAL PRODUCT DECLARATION OF ERIC BOISVERT OF MATROX ELECTRONIC SYSTEMS**
SYNOPSYS, INC., Plaintiff, vs. RICOH COMPANY, LTD., Defendant.	

I, Eric Boisvert, declare as follows:

1. I am the Vision Processor Product Line Supervisor of Matrox Electronic Systems, Ltd, for the Imaging division ("Matrox Electronic"). I have been an employee of Matrox Electronic since January 1994, and I am familiar with our operations and facilities from February 1997 to the present. I make this Declaration of my personal knowledge, and if called as a witness, I could and would testify competently to the statements contained herein.

2. Engineers at our company design application specific integrated circuits (ASICs). In designing ASICs, our engineers use various types of libraries in association with the Design Compiler® software from Synopsys.

3. We have used the following "Commercial ASICs" (using the specified technology libraries) as defined in the May 5, 2006 Amended Stipulation Re Supplemental Production In Accordance With Judge Chen's April 20, 2006 Order and Order Thereon (Ex. A):

#	PRODUCT	DESCRIPTION	LIBRARY	SYNTHESIZED IN U.S.
1	OASIS	Odyssey ASIC	Toshiba 0.14um	No
2	SIB	System interface bridge	Toshiba 0.14um	No
3	VIA/1	Video interface ASIC	AMI 0.35um	Did not undergo synthesis

4. The following product included on the original Declaration has been removed from the list above because, after further investigation, it was determined that it was synthesized prior to the damages period:

#	PRODUCT	DESCRIPTION	LIBRARY	REASON FOR REMOVAL
1	VIA/0	Video interface ASIC	LSI 0.5um	Synthesized prior to damages period

I declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct. This declaration was executed in Dorval, Quebec on May 10, 2006.

Eric Boisvert ing., M.Sc.A.

EXHIBIT A

Teresa M. Corbin (SBN 132360)
Denise M. De Mory (SBN 168076)
Jaclyn C. Fink (SBN 217913)
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Attorneys for Defendants AEROFLEX INCORPORATED, AEROFLEX COLORADO SPRINGS, INC., AMI SEMICONDUCTOR, INC., MATROX ELECTRONIC SYSTEMS, LTD., MATROX GRAPHICS, INC., MATROX INTERNATIONAL CORP., and MATROX TECH, INC.

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

RICOH COMPANY, LTD.,

Plaintiff,

vs.

AEROFLEX INCORPORATED, AMI SEMICONDUCTOR, INC., MATROX ELECTRONIC SYSTEMS LTD., MATROX GRAPHICS INC., MATROX INTERNATIONAL CORP., MATROX TECH, INC., AND AEROFLEX COLORADO SPRINGS, INC.,

Defendants.

Case No. C03-04669 MJJ (EMC)

AMENDED STIPULATION AND ORDER RE SUPPLEMENTAL PRODUCTION IN ACCORDANCE WITH JUDGE CHEN'S APRIL 20, 2006 ORDER ; ORDER THEREON

IT IS HEREBY STIPULATED AND AGREED by and between Ricoh Company, Ltd. ("Ricoh") and Aeroflex Incorporated, AMI Semiconductor, Inc., Matrox Electronics Systems, Ltd., Matrox Graphics Inc., Matrox International Corp., Matrox Tech., Inc. and Aeroflex Colorado Springs, Inc. (the "Defendants") that:

1. A "Commercial ASIC" is any ASIC (as defined in U.S. Patent No. 4,922,432 at Col. 1:13-17) that was, between 1997 and the present, (1) synthesized using Design Compiler for which (2) revenue was received and (3) one or more physical ASICs were manufactured (whether considered to

be a prototype or not). To avoid any doubt, all three criteria must be met and all three criteria must have occurred between 1997 and the present for an ASIC to qualify as a "Commercial ASIC."

2. Subject to the limitations set forth in the paragraphs below, the Defendants will identify and produce documents relating to Commercial ASICs synthesized between 1997 and the present by subsidiaries, including those ASICs for which synthesis was performed before acquisition of the subsidiary or its assets, for any Commercial ASIC either synthesized in the United States or sold in the United States, except that Commercial ASICs synthesized before an acquisition or asset purchase will not be identified if the acquiring party did not obtain rights to the ASICs. The Defendants will identify and produce documents, subject to the limitations set forth below, relating to Commercial ASICs synthesized by third parties provided that the synthesis was done at the request, direction or control of any named party.

3. For all newly identified products, Ricoh agrees to accept production of only "product packages" and financial information. The "product package" for a newly identified Commercial ASIC will include, to the extent it exists and is within the producing Defendant's possession, custody or control, the (1) script(s), including DC setup files, (2) inputs, including RTL inputs,[1] (3) technology library(ies), (4) log file(s) and (5) netlist(s) for the newly identified Commercial ASIC.

4. For all newly identified Commercial ASICs, the Defendants agree to produce financial documents including sales and cost information to the extent such information exists and is within the producing Defendant's possession, custody or control, with the following qualification: if all synthesis was done in the United States, or the RTL or technology library was supplied from the United States, or the netlist or mask data was shipped into the United States for manufacturing, then the producing Defendant will produce worldwide sales information for the newly identified Commercial ASIC. Otherwise, the producing Defendant will produce only information regarding sales in the United States.

---

[1] The Defendants shall determine whether any third party, non-Synopsys software (e.g., a flowchart translator) was used to convert an input specification to RTL. If so, the Defendants shall identify such third party software and produce the input specification and the converted RTL.

5. The Defendants will update their product declarations and library declarations (to the extent such updates are called for by newly identified ASICs) by May 10.

6. The Defendants will make good faith efforts to produce all documents by May 15. The product packages will be produced in an electronically searchable format. The financial documents will be produced in bates labeled and a native electronic format, to the extent such format exists.

7. To the extent that a particular Defendant does not have a complete product package or financial information for a newly identified ASIC, the Defendant will inform Ricoh that it does not have such information. To the extent the Defendant knows if such information is in the possession, custody, and control of a third party, it will identify such third party. To the extent that responsive information is the possession, custody or control of third parties known to the Defendants, the Defendants will cooperate in good faith in assisting Ricoh to obtain such information by requesting that the third party provide such information to it. Ricoh, however, understands that the Defendants' obligations under this Stipulation are limited to making good faith requests.

8. The Defendants will make good faith efforts to provide additional 30(b)(6) deponents before June 9. The Defendants will work in good faith to try to schedule depositions such that all or most of the 30(b)(6) deponents are produced in one location in a one week period.

9. This Stipulation resolves the issues raised by Ricoh's Motion for Sanctions filed on February 21, 2006. If the Defendants fail to perform in accordance with any of the terms of this Stipulation, Ricoh reserves the right to seek evidentiary, monetary, or other sanctions.

10. To the extent that new Commercial ASICs are identified, Ricoh and the Defendants agree that Ricoh's Final Infringement Contentions served on March 24, 2006 shall, in substantial part, satisfy Ricoh's obligations to produce Final Infringement Contentions with regard to the newly identified Commercial ASICs. Ricoh, however, shall supplement its Final Infringement Contentions for each newly identified Commercial ASIC by identifying only the inputs that satisfy the following elements of claim 13: "storing data describing a set of available integrated circuit hardware cells for performing the actions and conditions defined in the stored set" and "describing for a proposed application specific integrated circuit a series of architecture independent actions and conditions." To the extent that the Defendants produced declarations, documents, and deponents as set forth above,

Ricoh will provide this supplement on or before June 19, 2006. In the event that the above deadlines are not met, the parties will meet and confer in good faith regarding an appropriate time for supplementation.

Dated: May 5, 2006

HOWREY LLP

By: /s/ Denise M. De Mory
Attorneys for Defendants AEROFLEX INCORPORATED, AEROFLEX COLORADO SPRINGS, INC., AMI SEMICONDUCTOR, INC., MATROX ELECTRONIC SYSTEMS, LTD., MATROX GRAPHICS INC., MATROX INTERNATIONAL CORP. and MATROX TECH, INC.

Dated: May 5, 2006

DICKSTEIN SHAPIRO MORIN & OSHINSKY, LLP

By: /s/Kenneth W. Brothers
Kenneth W. Brothers (*pro hac vice*)

ALTSHULER, BERZON NUSSBAUM, RUBIN & DEMAIN
Jeffrey B. Demain
Attorneys for Plaintiff and Defendant RICOH COMPANY, LTD.

ORDER

Pursuant to stipulation, it is so ordered. ~~The continued hearing on Ricoh's Motion for Sanctions set for May 3, 2006 is hereby vacated.~~

This order ~~terminates Docket No. 358.~~ modifies the Order entered as Docket No. 448.

DATED: May 8, 2006

UNITED STATES DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA
IT IS SO ORDERED AS MODIFIED
Judge Edward M. Chen

PROOF OF SERVICE

STATE OF CALIFORNIA)
) ss.:
COUNTY OF SAN FRANCISCO)

I am employed in the County of San Francisco, State of California. I am over the age of 18 and not a party to the within action. My business address is 525 Market Street, Suite 3600, San Francisco, California 94105.

On May 10, 2006 I served on the interested parties in said action the within:

SECOND SUPPLEMENTAL PRODUCT DECLARATION OF ERIC BOISVERT OF MATROX ELECTRONIC SYSTEMS

by causing said document to be sent by Electronic Mail on May 10, 2006 to the email addresses indicated for the parties listed below and by placing a true copy thereof in a sealed envelope(s) addressed as stated below and causing such envelope(s) to be delivered as follows:

Gary M. Hoffman, Esq.
HoffmanG@dsmo.com
Dickstein Shapiro Morin & Oshinsky, LLP
2101 L Street, N.W.
Washington, DC 20037-1526

Facsimile No.: (202) 887-0689

Jeffrey Demain, Esq.
jdemain@altshulerberzon.com
Altshuler, Berzon, Nussbaum, Rubin & Demain
177 Post Street, Suite 300
San Francisco, CA 94108

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Edward A. Meilman, Esq.
MeilmanE@dsmo.com
Dickstein Shapiro Morin & Oshinsky, LLP
1177 Avenue of the Americas
New York, NY 10036-2714

Facsimile No.: (212) 896-5471

☒ (OVERNIGHT DELIVERY) on May 10, 2006 by depositing in a box or other facility regularly maintained by Federal Express, an express service carrier, or delivering to a courier or driver authorized by said express service carrier to receive documents, a true copy of the foregoing document in sealed envelopes or packages designated by the express service carrier, addressed as stated above, with fees for overnight delivery paid or provided for and causing such envelope(s) to be delivered by said express service carrier on.

I declare under penalty of perjury that I am employed in the office of a member of the bar of this Court at whose direction the service was made and that the foregoing is true and correct.

Executed on May 10, 2006, at San Francisco, California.

Peter L. Kasenenko
(Type or print name)

Peter L. Kasenenko
(Signature)

EXHIBIT 65

COPY

IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

RICOH COMPANY, LTD. Plaintiff, v. AEROFLEX INCORPORATED, AMI SEMICONDUCTOR, INC., MATROX ELECTRONIC SYSTEMS LTD., MATROX GRAPHICS INC., MATROX INTERNATIONAL CORP. and MATROX TECH, INC., Defendants.	)	C.A. No. 03-103

COMPLAINT

Plaintiff Ricoh Company, Ltd. ("Ricoh") for its Complaint against Defendants Aeroflex Incorporated ("Aeroflex"), AMI Semiconductor, Inc. ("AMI"), Matrox Electronic Systems Ltd. ("Matrox"), Matrox Graphics Inc. ("Matrox Graphics"), Matrox International Corp. ("Matrox Int'l"), and Matrox Tech, Inc. ("Matrox Tech"), alleges as follows:

PARTIES

1. Plaintiff Ricoh is a corporation organized under the laws of Japan and maintains its principal place of business at 3-6 1-chome, Nakamagome, Tokyo, Japan.

2. Upon information and belief, Defendant Aeroflex is a corporation organized under the laws of the State of Delaware, maintains its principal place of business at 35 S. Service Road, Plainview, NY, 11803, and has appointed The Corporation Trust Company, Corporation Trust Center, 1209 Orange Street, Wilmington, DE 19801 as its registered agent in Delaware.

3. Upon information and belief, Defendant AMI is a corporation organized under the laws of the State of Delaware, maintains its principal place of business at 2300 Buckskin Road,

Pocatello, ID 83201, and has appointed The Corporation Trust Company, Corporation Trust Center, 1209 Orange Street, Wilmington, DE 19801 as its registered agent in Delaware.

4. Upon information and belief, Defendant Matrox is a corporation organized under the laws of Quebec, Canada, maintains its principal place of business at 1055 Boul St-Regis, Dorval, Quebec H9P 2T4 Canada and is doing business in Delaware and/or has committed the acts complained of in Delaware.

5. Upon information and belief, Defendant Matrox Graphics is a corporation organized under the laws of Quebec, Canada, maintains its principal place of business at 1055 Boul St-Regis, Dorval, Quebec H9P 2T4 Canada and is doing business in Delaware and/or has committed the acts complained of in Delaware.

6. Upon information and belief, Defendant Matrox Int'l is a corporation organized under the laws of New York, maintains its principal place of business at 625 State Rt 3, Unit B, Plattsburgh, NY 12901, and is doing business in Delaware and/or has committed the acts complained of in Delaware.

7. Upon information and belief, Defendant Matrox Tech is a corporation organized under the laws of the State of Delaware, maintains its principal place of business at 1075 Broken Sound Parkway, NW, Boca Raton, FL 33487-3524 and has appointed The Corporation Trust Company, Corporation Trust Center, 1209 Orange Street, Wilmington, DE 19801 as its registered agent in Delaware.

JURISDICTION

8. This action arises under the patent laws of the United States, Title 35, United States Code, and more particularly under 35 U.S.C. §§ 271 et. seq.

9. This Court has subject matter jurisdiction over this patent infringement action under the Judicial Code of the United States, 28 U.S.C. §§ 1338(a) and 1331.

10. This Court has personal jurisdiction over the Defendants because Defendants are present and/or doing business in Delaware either directly or through their agents, or alternatively, are incorporated in Delaware.

VENUE

11. Venue is proper in this district pursuant to 28 U.S.C. § 1391 in that Defendants reside in this judicial district and/or a substantial part of the events or omissions giving rise to the claim occurred in this judicial district and/or are found in this judicial district and/or are aliens.

FACTUAL BACKGROUND

12. On May 1, 1990, the U.S. Patent and Trademark Office ("USPTO") duly and legally issued United States Letters Patent No. 4,922,432 (the " '432 Patent") in the names of Hideaki Kobayashi and Masahiro Shindo for their invention titled "Knowledge Based Method and Apparatus for Designing Integrated Circuits using Functional Specifications." A copy of the '432 Patent is attached hereto as Exhibit 1.

13. By assignment, Ricoh is the owner of the entire right, title, and interest in the '432 Patent and has the sole right to sue and recover for infringement thereof.

14. The '432 Patent describes, inter alia, a method for designing an application specific integrated circuit. By using the invention of the '432 Patent, one can define functional architecture independent specifications for an integrated circuit and translate functional architecture independent specifications into the detailed information needed for directly producing the integrated circuit.

PATENT INFRINGEMENT

COUNT 1

15. Ricoh repeats and realleges the allegations set forth in paragraphs 1 through 14 hereof.

16. Upon information and belief, Aeroflex has been and is now infringing the '432 Patent by using, offering to sell, and/or by selling and/or importing into the United States application specific integrated circuits designed by or using information generated by, the process of one or more of claims 13-20 of the '432 Patent, either literally or under the doctrine of equivalents.

17. Upon information and belief, Aeroflex will continue to infringe the '432 Patent unless enjoined by this Court.

18. As a consequence of Aeroflex's infringement, Ricoh has been irreparably damaged to an extent not yet determined, and Ricoh will continue to be irreparably damaged by such acts in the future unless Aeroflex is enjoined by this Court from committing further acts of infringement.

19. Upon information and belief, Aeroflex's infringement of the '432 Patent is willful.

20. Ricoh is entitled to recover damages adequate to compensate for Aeroflex's infringement.

COUNT 2

21. Ricoh repeats and realleges the allegations set forth in paragraphs 1 through 14 hereof.

22. Upon information and belief, AMI has been and is now infringing the '432 Patent by using, offering to sell, and/or by selling and/or importing into the United States application

specific integrated circuits designed by or using information generated by, the process of one or more of claims 13-20 of the '432 Patent, either literally or under the doctrine of equivalents.

23. Upon information and belief, AMI will continue to infringe the '432 Patent unless enjoined by this Court.

24. As a consequence of AMI's infringement, Ricoh has been irreparably damaged to an extent not yet determined, and Ricoh will continue to be irreparably damaged by such acts in the future unless AMI is enjoined by this Court from committing further acts of infringement.

25. Upon information and belief, AMI's infringement of the '432 Patent is willful.

26. Ricoh is entitled to recover damages adequate to compensate for AMI's infringement.

COUNT 3

27. Ricoh repeats and realleges the allegations set forth in paragraphs 1 through 14 hereof.

28. Upon information and belief, Matrox has been and is now infringing the '432 Patent by using, offering to sell, and/or by selling and/or importing into the United States application specific integrated circuits designed by or using information generated by, the process of one or more of claims 13-20 of the '432 Patent, either literally or under the doctrine of equivalents.

29. Upon information and belief, Matrox will continue to infringe the '432 Patent unless enjoined by this Court.

30. As a consequence of Matrox's infringement, Ricoh has been irreparably damaged to an extent not yet determined, and Ricoh will continue to be irreparably damaged by such acts

in the future unless Matrox is enjoined by this Court from committing further acts of infringement.

31. Upon information and belief, Matrox's infringement of the '432 Patent is willful.

32. Ricoh is entitled to recover damages adequate to compensate for Matrox's infringement.

COUNT 4

33. Ricoh repeats and realleges the allegations set forth in paragraphs 1 through 14 hereof.

34. Upon information and belief, Matrox Graphics has been and is now infringing the '432 Patent by using, offering to sell, and/or by selling and/or importing into the United States application specific integrated circuits designed by or using information generated by, the process of one or more of claims 13-20 of the '432 Patent, either literally or under the doctrine of equivalents.

35. Upon information and belief, Matrox Graphics will continue to infringe the '432 Patent unless enjoined by this Court.

36. As a consequence of Matrox Graphics' infringement, Ricoh has been irreparably damaged to an extent not yet determined, and Ricoh will continue to be irreparably damaged by such acts in the future unless Matrox Graphics is enjoined by this Court from committing further acts of infringement.

37. Upon information and belief, Matrox Graphics' infringement of the '432 Patent is willful.

38. Ricoh is entitled to recover damages adequate to compensate for Matrox Graphics' infringement.

COUNT 5

39. Ricoh repeats and realleges the allegations set forth in paragraphs 1 through 14 hereof.

40. Upon information and belief, Matrox Int'l has been and is now infringing the '432 Patent by using, offering to sell, and/or by selling and/or importing into the United States application specific integrated circuits designed by or using information generated by, the process of one or more of claims 13-20 of the '432 Patent, either literally or under the doctrine of equivalents.

41. Upon information and belief, Matrox Int'l will continue to infringe the '432 Patent unless enjoined by this Court.

42. As a consequence of Matrox Int'l's infringement, Ricoh has been irreparably damaged to an extent not yet determined, and Ricoh will continue to be irreparably damaged by such acts in the future unless Matrox Int'l is enjoined by this Court from committing further acts of infringement.

43. Upon information and belief, Matrox Int'l's infringement of the '432 Patent is willful.

44. Ricoh is entitled to recover damages adequate to compensate for Matrox Int'l's infringement.

COUNT 6

45. Ricoh repeats and realleges the allegations set forth in paragraphs 1 through 14 hereof.

46. Upon information and belief, Matrox Tech has been and is now infringing the '432 Patent by using, offering to sell, and/or by selling and/or importing into the United States

application specific integrated circuits designed by or using information generated by, the process of one or more of claims 13-20 of the '432 Patent, either literally or under the doctrine of equivalents.

47. Upon information and belief, Matrox Tech will continue to infringe the '432 Patent unless enjoined by this Court.

48. As a consequence of Matrox Tech's infringement, Ricoh has been irreparably damaged to an extent not yet determined, and Ricoh will continue to be irreparably damaged by such acts in the future unless Matrox Tech is enjoined by this Court from committing further acts of infringement.

49. Upon information and belief, Matrox Tech's infringement of the '432 Patent is willful.

50. Ricoh is entitled to recover damages adequate to compensate for Matrox Tech's infringement.

PRAYER FOR RELIEF

WHEREFORE, Ricoh prays for entry of judgment:

A. that Aeroflex has infringed the '432 Patent;

B. that Aeroflex, its agents, employees, representatives, successors, and assigns and those acting, or purporting to act, in privity or in concert with Aeroflex, be preliminarily and permanently enjoined from further infringement of the '432 Patent;

C. that Aeroflex account for and pay to Ricoh all damages under 35 U.S.C. § 284, including enhanced damages, caused by the infringement of the '432 Patent, and attorneys' fees pursuant to 35 U.S.C. § 285;

D. that Ricoh be granted pre-judgment and post-judgment interest on the damages

caused to it by reason of Aeroflex's infringement of the '432 Patent;

E. that AMI has infringed the '432 Patent;

F. that AMI, its agents, employees, representatives, successors, and assigns and those acting, or purporting to act, in privity or in concert with AMI, be preliminarily and permanently enjoined from further infringement of the '432 Patent;

G. that AMI account for and pay to Ricoh all damages under 35 U.S.C. § 284, including enhanced damages, caused by the infringement of the '432 Patent, and attorneys' fees pursuant to 35 U.S.C. § 285;

H. that Ricoh be granted pre-judgment and post-judgment interest on the damages caused to it by reason of AMI's infringement of the '432 Patent;

I. that Matrox has infringed the '432 Patent;

J. that Matrox, its agents, employees, representatives, successors, and assigns and those acting, or purporting to act, in privity or in concert with Matrox, be preliminarily and permanently enjoined from further infringement of the '432 Patent;

K. that Matrox account for and pay to Ricoh all damages under 35 U.S.C. § 284, including enhanced damages, caused by the infringement of the '432 Patent, and attorneys' fees pursuant to 35 U.S.C. § 285;

L. that Ricoh be granted pre-judgment and post-judgment interest on the damages caused to it by reason of Matrox's infringement of the '432 Patent;

M. that Matrox Graphics has infringed the '432 Patent;

N. that Matrox Graphics, its agents, employees, representatives, successors, and assigns and those acting, or purporting to act, in privity or in concert with Matrox Graphics, be preliminarily and permanently enjoined from further infringement of the '432 Patent;

O. that Matrox Graphics account for and pay to Ricoh all damages under 35 U.S.C. § 284, including enhanced damages, caused by the infringement of the '432 Patent, and attorneys' fees pursuant to 35 U.S.C. § 285;

P. that Ricoh be granted pre-judgment and post-judgment interest on the damages caused to it by reason of Matrox Graphics' infringement of the '432 Patent;

Q. that Matrox Int'l has infringed the '432 Patent;

R. that Matrox Int'l, its agents, employees, representatives, successors, and assigns and those acting, or purporting to act, in privity or in concert with Matrox Int'l, be preliminarily and permanently enjoined from further infringement of the '432 Patent;

S. that Matrox Int'l account for and pay to Ricoh all damages under 35 U.S.C. § 284, including enhanced damages, caused by the infringement of the '432 Patent, and attorneys' fees pursuant to 35 U.S.C. § 285;

T. that Ricoh be granted pre-judgment and post-judgment interest on the damages caused to it by reason of Matrox Int'l's infringement of the '432 Patent;

U. that Matrox Tech has infringed the '432 Patent;

V. that Matrox Tech, its agents, employees, representatives, successors, and assigns and those acting, or purporting to act, in privity or in concert with Matrox Tech, be preliminarily and permanently enjoined from further infringement of the '432 Patent;

W. that Matrox Tech account for and pay to Ricoh all damages under 35 U.S.C. § 284, including enhanced damages, caused by the infringement of the '432 Patent, and attorneys' fees pursuant to 35 U.S.C. § 285;

X. that Ricoh be granted pre-judgment and post-judgment interest on the damages caused to it by reason of Matrox Tech's infringement of the '432 Patent;

Y. that costs be awarded to Ricoh; and

Z. that Ricoh be granted such other and further relief as the Court may deem just and proper under the current circumstances.

by Lk/dw (4025)

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Dated: January 21, 2003

EXHIBIT 66

INTERNATIONAL JOURNAL OF COMPUTER AIDED VLSI DESIGN

VOLUME 1
NUMBER 4

SPECIAL ISSUE: PART 2
VLSI CAD IN JAPAN

ABLEX PUBLISHING
CORPORATION
NORWOOD, NEW JERSEY

International

Journal of Computer Aided VLSI Design

Volume 1, Number 4, 1989

SPECIAL ISSUE: Part II

VLSI CAD IN JAPAN

Hideaki Kobayashi, Guest Editor

CONTENTS

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Volume 1, Number 4, 1989

SPECIAL ISSUE: Part II

VLSI CAD IN JAPAN

Hideaki Kobayashi, Guest Editor

CONTENTS

Regular Contribution

Book Review:

International Journal of Computer Aided VLSI Design 1, 351–355 (1989)

Part II
Guest Editorial

HIDEAKI KOBAYASHI

Application-specific integrated circuit (ASIC) users in Japan are mainly "set makers" (system designers) who are not experts in VLSI design. They use (TTL) transistor-transistor logic–based techniques to design logic circuits (or netlists). Test vectors often are not generated by ASIC users. Many circuits designed by ASIC users do not implement initial chip functions. This often results in problems associated with design responsibilities between ASIC users and semiconductor makers.

With advanced CAD tools and systems, the interface between ASIC users and semiconductor makers will be shifted to a higher functional level. ASIC users can enter desired chip functions using optimum input forms such as truth tables, state diagrams, flowcharts, and hardware description languages (HDLs). ASIC users can also ensure initial chip functions without generating test vectors at a structural (circuit) level. Chips can be developed by ASIC users who are not familiar with circuit design or semiconductor technology.

Automatic translation between behavioral or functional inputs to logic circuits is provided by logic synthesis systems. There are two different types of approaches to automatic logic synthesis: algorithmic and rule-based. IF–THEN-type rules rather than algorithmic programming languages are used in the latter approach to synthesize logic circuits. These rules are extracted from expert ASIC designers who have been designing chips for many years.

Many Japanese semiconductor makers have developed in-house software for logic synthesis. A variety of commercial software for logic synthesis is also available in the Japanese market. Table 1 shows an example list of commercial software for logic synthesis. Table 2 shows an example list of in-house software for logic synthesis. These tables are translated from the article entitled "Logic Synthesis Software for ASIC Makes Design at the Functional Level Possible" by U. Kojima, published in *Nikkei Electronics*, November 1988 issue. Target applications of ASICs designed by these logic synthesis systems include audio visual machines, communications large-scale integration (LSI), digital signal processors, general-purpose microprocessors, micro program control, office automation, and peripheral LSI.

A list of other logic synthesis systems is provided in Table 3. These systems perform synthesis by translating a functional (algorithmic) description into a structural (data path and controller) description. They are compared in the second article of this special issue.

Table 1. Commercial Logic Synthesis Software

Name:	ZEPHCAD
Vendor:	Fujitsu Ltd.
Input form:	State diagram, Boolean expression, truth table
Design style:	CMOS gate array, CMOS standard cell
Name:	PARTHENON
Vendor:	NTT Data Communications Systems Corporation
Input form:	HDL (SFL)
Design style:	CMOS gate array, CMOS standard cell
Name:	Logic Synthesizer
Vendor:	LSI Logic Corporation
Input form:	State diagram, Truth table, Boolean expression, parameter
Design style:	CMOS gate array, CMOS standard cell
Name:	Finesse
Vendor:	Seattle Silicon Corporation
Input form:	Truth table, Boolean expression, state diagram
Design style:	CMOS standard cell
Name:	Logic Compiler
Vendor:	Silicon Compiler Systems Corporation
Input form:	Boolean expression, truth table, functional diagram, state diagram, HDL
Design style:	CMOS standard cell
Name:	SilcSyn
Vendor:	Silc Technologies, Inc.
Input form:	HDL (DDL)
Design style:	CMOS gate array, CMOS standard cell
Name:	Logic Consultant
Vendor:	Trimeter Technologies Corporation
Input form:	Boolean expression, netlist
Design style:	CMOS gate array
Name:	Design Compiler
Vendor:	Synopsys, Inc.
Input form:	HDL (Verilog), Boolean expression, truth table, netlist
Design style:	CMOS gate array, CMOS standard cell
Name:	State Machine Compiler
Vendor:	VLSI Technology, Inc.
Input form:	Boolean expression, truth table, parameter, state diagram, netlist, functional diagram, HDL (VHDL)
Design style:	CMOS gate array, CMOS standard cell

Table 2. In-House Logic Synthesis Software

Name:	FLORA
Company:	Fujitsu, Ltd.
Input form:	Functional diagram
Results:	Over 100 chips
Name:	ProLogic
Company:	Hitachi, Ltd.
Input form:	Structural and behavioral description of datapath and control circuits
Results:	Several samples under evaluation
Name:	LODES
Company:	Matsushita Electric Industrial Co., Ltd.
Input form:	Functional diagram, Boolean expression, truth table, HDL (HSL-FX)
Results:	Two chips for practical use
Name:	TL/C
Company:	Matsushita Electric Industrial Co., Ltd.
Input form:	Circuit diagram, Boolean expression, truth table, state diagram
Results:	Evaluation completed
Name:	LORES/EX
Company:	Mitsubishi Electric Corp.
Input form:	Functional diagram
Results:	Under evaluation
Name:	Fusion
Company:	NEC Corp.
Input form:	HDL (FDL)
Results:	Two chips
Name:	EXLOG
Company:	NEC Corp.
Input form:	HDL (FDL)
Results:	One chip
Name:	ANGEL
Company:	NEC Corp.
Input form:	HDL (HSL-FX)
Results:	Two chips
Name:	CLS
Company:	Oki Electric Industry Co., Ltd.
Input form:	HDL (HSL-FX)
Applications:	Microprocessors, DSP, control LSI
Results:	Five chips
Name:	Logic Synthesis System
Company:	Sharp Corp.
Input form:	Boolean expression, truth table, functional diagram
Results:	Under evaluation
Name:	Logic Synthesis Systems
Company:	Toshiba Corp.
Input form:	HDL (HHDL)
Results:	Thirty chips

Table 3. Other Logic Synthesis Software

Name:	CMU-DA System
Company:	Carnegie-Mellon University
Input form:	IPS language
Results:	Not available
Name:	VLSI Design Automation Assistant
Company:	AT&T Bell Laboratories
Input form:	ISPS language
Results:	Several digital systems
Name:	ALERT
Company:	IBM Watson Research Center
Input form:	Iverson's APL
Results:	Not available
Name:	Flamel
Company:	Stanford University
Input form:	Pascal
Results:	Not available
Name:	KBSC
Company:	Ricoh–International Chip Corporation
Input form:	Flowchart
Results:	Ten chips

The first article is "Unified Hardware Description Language and Its Support Tools" from Fujitsu Laboratories Ltd. A new hardware description language called UHDL (Unified Hardware Description Language) is proposed to describe asynchronous behavior and to synthesize large circuits. A hierarchical structure can be described by UHDL from several viewpoints, such as behavior, interface, and data paths.

The second article is "KBSC: A Knowledge-Based Approach to Automatic Logic Synthesis" from International Chip Corporation and Ricoh Company. A knowledge-based silicon compiler (KBSC) provides users with a front-end graphic interface to automatic logic synthesis. Both data-path and control circuits are synthesized by using rules extracted from expert ASIC designers. KBSC's flowchart input form allows ASIC users to enter desired chip functions easily, and verify these functions to ensure functional correctness.

The third article is "Development and Evaluation of an Architecture Design System for Application-Specific Integrated Circuits" from Waseda University. In this article, automatic architecture synthesis for special-purpose integrated circuits is discussed. The authors suggest that their system can synthesize and modify an initial circuit from a given algorithm. Target architectures are small- to medium-scale integrated circuits and are used to implement algorithms for digital signal processing.

The precise analysis of submicron pattern imaging becomes more important as feature sizes decrease. The minimum feature size of a 16-Mbit dynamic random-access memory is approximately half-microns. The fourth article is "A Novel Fast Calculation Method for Partial Coherent Images with Optical Aberration and Its Application to Submicron Pattern Imaging" from

Hitachi Ltd. This method calculates images of isolated square and isolated elbow mask patterns with various optical aberrations. It also calculates image distortions with several types of aberrations simultaneously.

Hideaki Kobayashi Dr. Kobayashi received both M.S. and Ph.D. degrees in Electrical Engineering from Waseda University, Tokyo, Japan. He joined the Department of Electrical and Computer Engineering at the University of South Carolina in 1980, where he is currently an Associate Professor. He is also Director of the VLSI/AI Design Laboratory at the Center for Machine Intelligence located at the new Swearingen Engineering Center, which is one of the most advanced facilities of its kind in the world. His current research interests include VLSI architecture for AI applications and knowledge-based silicon compilation. In addition to teaching on campus, his VLSI courses also are taught throughout the United States via the National Technological University.

International Chip Corporation was established in 1985 in Columbia, South Carolina as culmination of over ten years of research by Dr. Kobayashi, one of the two principals in the firm who also serves as Chairman of the Board. Since 1986 the company has funded continuing research at the University of South Carolina in a private-public partnership with Carolina Research and Development Foundation. For-profit business applications and related product development are conducted at International Chip Corporation's corporate headquarters, within walking distance of the main campus of the University of South Carolina.

Dr. Kobayashi has published over 50 professional papers in leading United States, Japanese, and European journals. He serves as an Associate Editor of the International Journal of Computer Aided VLSI Design. He is frequently invited to speak at professional meetings and seminars relating to ASIC (application specific integrated circuit) design, VLSI CAD, knowledge-based systems, and other associated topics. He also has been the recipient of research grants from several sources, including the National Science Foundation and the Semiconductor Research Corporation. His career contributions have been recognized in several ways, including selection as one of the Outstanding Young Men of America for 1985. He is a member of IEEE and Eta Kappa Nu.

EXHIBIT 68

Chart of Synopsys-Ricoh Contracts

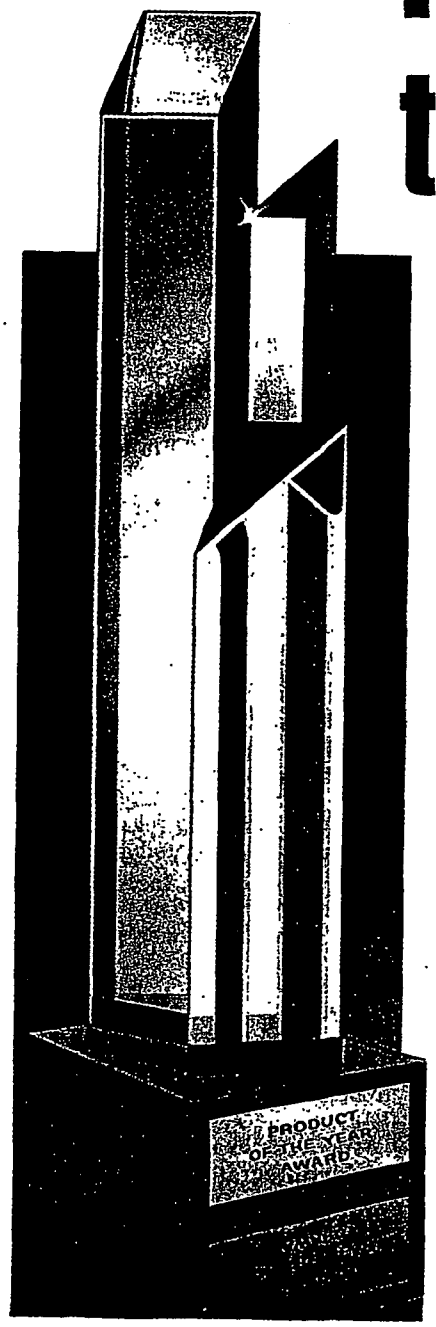
Contract #	Date	Bates Range	Relevant Synopsys Products	Company	Internal Doc #
SYNM-90-0053	6/1/1990	2SP0708268-2SP0708273	DC, HDL Compiler - Verilog	SHC	
SYN-90-0053	10/22/1990	2SP0708274-2SP0708287	DC, HDL Compiler - Verilog	SHC	
SYNM-91-0121	10/1/1991	2SP0708294-2SP0708299	DC, HDL Compiler - Verilog	SHC	
SYN-91-0121	10/1/1991	2SP0708300-2SP07083.13	DC, HDL Compiler - Verilog		
SYNR-91-0143	5/21/1991	2SP0708288-2SP0708293	DC, HDL Compiler - Verilog	SHC	
SYNM-92-0289	9/1/1992	2SP0708328-2SP0708332	DC, VHDL Compiler	NSKK	
SYN-92-0289	9/1/1992	2SP0708333-2SP0708344	DC, VHDL Compiler	NSKK	
SYN-93-0275	8/1/1993	2SP0708437-2SP0708447	DC-Expert, HDL Compiler – Verilog	NSKK	rl-3153
SYNM-93-0275	8/1/1993	2SP0708448-2SP0708452	DC, HDL Compiler - Verilog	NSKK	rl-0273
SYNM-93-0276	4/4/1993	2SP0708324-2SP0708327	DC, HDL Compiler - Verilog	NSKK	rl-1473
SYN-93-0276	4/4/1993	2SP0708314-2SP0708323	DC, HDL Compiler - Verilog	NSKK	rl-1024
SYNR-93-0356	3/19/1993	2SP0708345-2SP0708347	DC, HDL Compiler – Verilog, VHDL Compiler	NSKK	
SYNM-93-0364	4/1/1993	2SP0708348-2SP0708351	DC-Expert, HDL Compiler – Verilog, VHDL Compiler	NSKK	
SYN-93-0364		2SP0708352-2SP0708362	DC-Expert, HDL Compiler – Verilog, VHDL Compiler	NSKK	
SYN-93-0405	3/20/1993	2SP0708363-2SP0708374; 2SP0708388-2SP0708397	DC-Expert, HDL Compiler – Verilog	NSKK	rc-29A3
SYNR-93-0405	4/16/1993	2SP0708380-2SP0708382	DC-Expert, HDL Compiler – Verilog	NSKK	
SYNM-93-0405		2SP0708383-2SP0708387	DC-Expert, HDL Compiler – Verilog	NSKK	
SYN-93-0478	9/10/1993	2SP0708422-2SP0708433	DC-Expert, HDL Compiler – Verilog, VHDL Compiler	NSKK	rc-3083
SYNR-93-0478	12/7/1993	2SP0708434-2SP0708436	DC-Expert, HDL Compiler – Verilog, VHDL Compiler	NSKK	29B3
SYNR-93-0472	6/1/1993	2SP0708405-2SP0708416	DC-Expert, HDL Compiler – Verilog, Design Ware Developer, VHDL Compiler	NSKK	2674
SYNM-93-0478	9/27/1993	2SP0708417-2SP0708421	DC-Expert, HDL Compiler – Verilog, VHDL Compiler	NSKK	rc-0193

SYNR-93-0497	10/1/1993	2SP0708453-2SP0708455	DC, VHDL Compiler	NSKK	Ricoh-2093
SYN-93-0507	10/18/1993	2SP0708200 - 2SP0708210	DC-Expert, HDL Compiler – Verilog	NSKK	rc-15A3
SYNM-93-0507	10/18/1993	2SP0708211-2SP0708215	DC-Expert, HDL Compiler – Verilog	NSKK	2c-2793
SYNMO-94-0405	4/16/1993	2SP0708375	DC-Expert, HDL Compiler – Verilog	NSKK	
SYNR-94-0405	6/15/1994	2SP0708376-2SP0708379	DC-Expert, DC-Professional, HDL Compiler – Verilog	NSKK	954
SYNM-94-0497	1/26/1994	2SP0708456-2SP0708460	DC-Expert, HDL Compiler – Verilog, VHDL Compiler	NSKK	rc-1014
SYN-94-0497	1/26/1994	2SP0708461-2SP0708471	DC-Expert, HDL Compiler – Verilog, VHDL Compiler	NSKK	rc-1014
SYNM-94-0597	6/7/1994	2SP0708237-2SP0708241	DC-Expert, HDL Compiler – Verilog	NSKK	rc-2744
SYN-94-0597	6/7/1994	2SP0708242-2SP0708251	DC-Expert, HDL Compiler – Verilog	NSKK	rc-2744
SYNM-95-0871	10/27/1995	2SP0708231-2SP0708236	DC-Expert, DC-Professional, HDL Compiler – Verilog	NSKK	rl-12A5
SYN-95-0871	10/27/1995	2SP0708216-2SP0708226	DC-Expert, DC-Professional, HDL Compiler – Verilog, VHDL Compiler	NSKK	12A5
SYNR-96-0871-2	10/29/1996	2SP0708227-2SP0708230	DC-Expert, DC-Professional, HDL Compiler – Verilog, VHDL Compiler	NSKK	3096
SYNR-96-0871L-2	9/3/1996	2SP0708252-2SP0708253	DC-Expert, DC-Professional, HDL Compiler – Verilog, VHDL Compiler	NSKK	2826
SYNR-96-0871	3/12/1996	2SP0708254-2SP0708256	DC-Expert, DC-Professional, HDL Compiler – Verilog	NSKK	2126
SYN-96-1208	5/14/1996	2SP0708258-2SP0708267	DC-Expert, HDL Compiler – Verilog		
SYNR-96-1208L	9/25/1996	2SP0708257		NSKK	1996
SYNR-96-0472-2	1/21/1996	2SP0708398-2SP0708401	DC-Expert, HDL Compiler – Verilog, Design Ware Developer, VHDL Compiler	NSKK	1937
SYNR-96-0472	9/30/1996	2SP0708402-2SP0708404	DC-Expert, HDL Compiler – Verilog, Design Ware Developer, VHDL Compiler	NSKK	1996
SYNR-96-0497	3/25/1996	2SP0708472-2SP0708474	DC-Expert, HDL Compiler – Verilog, VHDL Compiler	NSKK	1936
SYNR-96-0497-2	3/28/1996	2SP0708475-2SP0708477	DC-Expert, HDL Compiler – Verilog, VHDL Compiler	NSKK	2636
NL-02811	5/22/1995	2SP0708478-2SP0708485	N/A – End User License Agreement	Synopsys	9404
NS-02811	5/22/1995	2SP0708486-2SP0708489	Support Agreement	Synopsys	
Certificate of Discontinued Use	10/28/2004	2SP0708705-2SP0708706	DC-Expert, DC-Ultra, HDL Compiler - Verilog	NSKK	

of Synopsys Products					

EXHIBIT 71

14th Annual Product of the Year Awards



From the thousands of products introduced in 1989, *Electronic Products* has chosen the most outstanding. The selections are based on significant advances in technology or its application, a decided innovation in design, or a substantial gain in price-performance.

As usual, picking winners was made difficult by the many impressive products announced during the year.

Here, then, are the 1989 award winners.

The HDL Compiler
Synopsys, Inc.
Mountain View, CA

RC224AT Full-duplex, V.22 bis 2,400-Bit/s Modem
Rockwell International Corp.
Semiconductor Products Div.
Newport Beach, CA

IDX Cable
W.L. Gore & Associates, Inc.
Phoenix, AZ

TLC2654 Chopper-stabilized Op Amp
Texas Instruments, Inc.
Dallas, TX

ML4812 Power Factor Controller IC
Micro Linear, San Jose, CA

Bak▲Pak™ High-frequency Burn-in System
EJ Systems, Inc.
Lawrence, MA

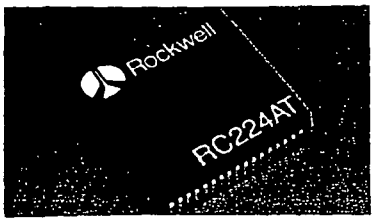
i860 RISC Microprocessor
Intel Corp., Santa Clara, CA

The Wafer Stack Storage Disk
Anamartic Inc., San Jose, CA

FC110 Fuzzy Logic Chip
Togai InfraLogic, Inc.
Irvine, CA

SP04649

Product of the Year Awards



The Rockwell International RC224AT full-duplex, V.22 bis modem with AT command set is the first single-chip modem that is truly a single chip.

peripherals to handle functions like AT command interpretation. It has an embedded 16C450 IBM PC-compatible UART that takes the place of an external UART for parallel-bus PC card modems. The RC224AT also supports serial-box modem applications through a V.24 RS-232-C serial host interface.

On top of all that, the RC224AT typically dissipates only 305 mW (530 mW max). And when inactive, the modem automatically shifts to a 37-mW sleep mode. This makes it particularly attractive for laptop computer and other battery-powered applications. ($28 ea/10,000.)

Rockwell International Corp.
Semiconductor Products Div.
Newport Beach, CA
Ralph Bond 714-833-6849
EEM FILE 3130 ▶ **CIRCLE 301**

IDC nears coaxial

Insulation displacement connector cable approaches the performance of coaxial cables at far less cost

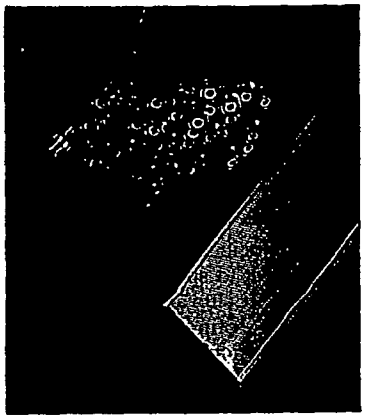
Innovations in the world of cable tend to be few and far between. But in 1989, W.L. Gore & Associates made a great stride with its IDX cable. This specially constructed cable terminates with standard 0.050-in. center insulation displacement connectors, like a ribbon cable. But the cable's performance almost matches that of far more expensive coaxial cables.

The IDX cable replaces a number of discrete coaxial cables, which must be terminated individually with bulky, costly SMA connectors. Termination of the IDX cable typically takes under 10 minutes. The cable is intended for use where near-coaxial performance and termination of many signals is needed, such as in video busing and switching systems.

Like coaxial cable, IDX cable has center signal-carrying conductors (either 28 or 30 AWG gauge) and a shielded outer conductor, which is connected to ground. But Gore goes a step further by surrounding each of these conductors with a dielectric material of expanded PTFE (polytetrafluoroethylene). This low-dielectric material maintains a controlled impedance between each signal wire and shield. It also keeps the cable thin enough so it can be terminated with insulation displacement connectors.

An outer insulation layer encases the entire cable. Prior to termination, the user removes part of the cable's shield to expose the core of the cable for termination. Drain or ground wires can be placed anywhere in the cable and terminated the same time as the signal conductors.

Signal crosstalk for the IDX cable is 3% to 5%, slightly higher than a coaxial cable but far less than a conventional IDC ribbon cable. Termination cost is about $6 to $10 for both



The IDX cable from W.L. Gore combines the mass termination ease and low termination cost of a ribbon cable with performance rivaling coaxial cables.

cable ends. The flexible cable is available in both 50- and 75-Ω impedances. ($0.40 to $0.80 per conductor ft, depending on volume.)

W.L. Gore & Associates, Inc.
Phoenix, AZ
Jim Ainsworth 602-431-0077
EEM FILE 6000 ▶ **CIRCLE 302**

Synthesis tool becomes de facto standard

Compiler translates ASIC designs from HDL to gate level

ASIC designers finally have at their fingertips a compiler that quickly translates a design from a hardware description language (HDL) to a gate-level ASIC implementation. The Synopsys HDL Compiler takes a task that has traditionally taken man-weeks or man-months and reduces it to minutes or hours of CPU time.

Designers have so enthusiastically embraced the HDL Compiler that it has become a de facto standard, with a number of simulation and ASIC vendors having formed partnerships with Synopsys (see *box*). That's not surprising, since the compiler supports two HDLs that are themselves de facto standards: the Gateway Design Automation* Verilog HDL and the Defense Department-mandated

SP04650

Product of the Year Awards

VHSIC HDL (VHDL).

On its own, the HDL Compiler completes the translation half of the logic synthesis process. To optimize their ASICs, designers combine the HDL Compiler with the Synopsys Design Compiler. They can thus minimize logic and optimize designs with respect to speed, area, loading, and an ASIC library. And because they have defined their ASIC designs in Verilog HDL or VHDL, designers can validate alternative architectures and make design tradeoffs.

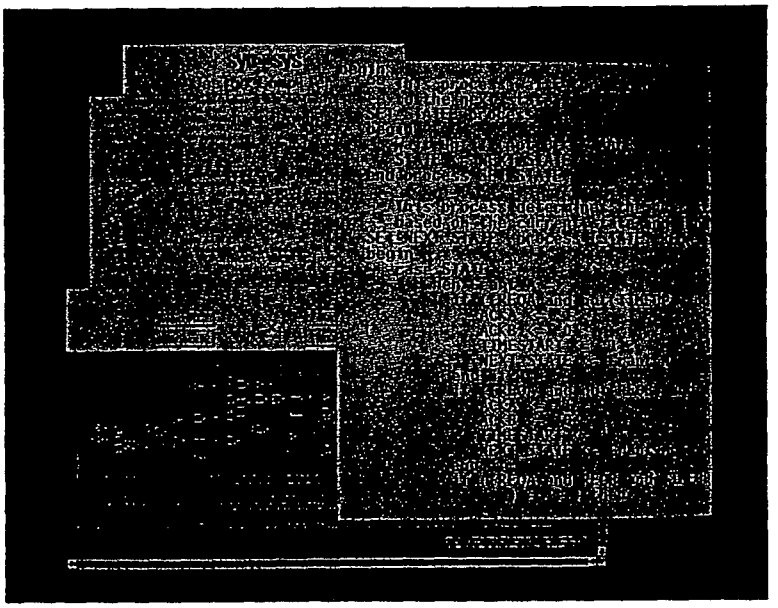
VHDL PARTNERSHIPS

Simulation Suppliers
- Gateway Design Automation
- Genrad
- MCC
- Vantage
- Zycad

ASIC Vendors
- Harris Semiconductor
- National Semiconductor
- LSI Logic

Gateway is now part of Cadence

Once designers have synthesized register-transfer-level circuit descriptions in one of the two HDLs with the HDL Compiler/Design Compiler, the optimized ASIC design is written out in VHDL or Verilog netlist format for gate-level verification.



The new VHDL option to the Synopsys HDL Compiler, used with the Design Compiler, can read in existing design descriptions.

Users can thus perform functional simulation at the RTL level, synthesize a gate-level netlist, and verify the functionality and performance of the design, all with the same vectors.

The VHDL synthesis capability could go a long way in bringing VHDL from a DOD mandate, presently confined to design specification and documentation, to acceptance as a standard language for exploring design alternatives and optimizing ASICs. (HDL Compiler with Verilog, $17,700; with VHDL option, $22,500.)

Synopsys, Inc.
Mountain View, CA
Bob Smith 415-962-5000
EEM FILE 2050 ▶ **CIRCLE 303**

Superchip breaks tradition

Intel's foray into RISC is a real break with the past. It may lead to low-cost workstations, as well as powerful multiprocessor installations

Intel's foray into RISC represents a real break with the past. It may lead to low-cost workstations, as well as powerful multiprocessor installations

The first of three dramatic microprocessor announcements made last year by Intel, the i860 represented a real architectural departure for the company. In contrast, the i486 was what everyone expected and the superscalar i960 has a family tree. All three made use of Intel's internal tools to develop complex chips from relatively high-level designs, and all three carry on multiple operations on chip, reducing pin traffic.

What makes the i860 stand out is its ability to handle numerics, both floating-point and integer, with enormous internal bus capacity. The path from the data cache to the floating-point control is 128 bits wide. The current 33-MHz version does over eight double-precision Linpacks without an external cache.

The i860 was first described in a paper presented at the International Solid State Circuits Conference in New York, and announced as a product shortly thereafter. The preliminary abstract for the ISSCC paper called it a coprocessor, and marketing people for other RISC processors have had a field day calling it that ever since. Intel, however, insists it is a standalone microprocessor, and is porting a multiprocessing Unix V.4 to it.

Standalone or not, its handling of floating-point numerics and its on-

EXHIBIT 73

Avant! Shakes Up Front-End Design - Jupiter CAE software - Product Announcement

Electronic News, June 21, 1999 by Ann Steffora

Scottsdale, Ariz.-Avant! Corp., Fremont, Calif., last week charged into the great submicron land grab with the announcement of Jupiter, a new product that the company is billing as a complete front-end design creation tool.

With the announcement, Avant! becomes just the latest EDA vendor to cater to OEMs' need to retool for deep submicron designs. The lead up to this week's 36th Annual Design Automation Conference in New Orleans has seen a number of companies introduce tools that consider the physical effects of design decisions early in the planning stage to reduce cycle times. The companies are hoping these capabilities will lure business away from competitors during the submicron transition.

Avant!'s Jupiter is positioned to compete directly with the Chip Architect product from Mountain View, Calif.,-based Synopsys Inc. As its foundation, Chip Architect uses Physical Synthesis, which is the incorporation of physical data in the early design planning stages for early timing prediction. Cadence Design Systems Inc., San Jose, also is said to be preparing its approach to deep-submicron, high-level design planning.

Avant! said its approach to the front end is different from the competition because, as in its other deep-submicron design tools, the company's Milkyway database serves as the backbone for Jupiter. The use of Milkyway eliminates the need for complex interfaces between tools, Avant! said.

Jupiter also contains a synthesis capability, which has spurred speculation that Jupiter could pose a challenge to Synopsys' Design Compiler tool. However, Avant! is not immediately planning to market Jupiter as a Design Compiler replacement, said Michael Jackson, head of product management for Avant!.

Synopsys' Design Compiler still leads the synthesis market with 81 percent market share in 1997, according to the market research firm Dataquest, San Jose. Even if Avant!'s technology proves to be as formidable as it asserts, unseating Synopsys may not likely occur for a number of years.

Although not the immediate plans, observers believe this is the direction Avant! will take, since best results are obtained by using the integrated synthesizer in Jupiter. The real question is whether OEMs will buy into the strategy.

Industry experts are not so excited about Avant!'s stance.

"The message is that, of course you can use Design Compiler, but it won't work as well," said Gary Smith, chief analyst of worldwide EDA at Dataquest. "Probably more important is how many engineers will drop their Cadence or Synopsys simulator. Design libraries are really tied to your simulator. To use Jupiter, the RTL tool flow has to be changed completely and there's not a lot of chance that will happen."

While a silicon vendor will adopt anything in order to get more (and bigger) designs in the door, unfortunately, unlike the IC CAD world, engineers buy CAE tools. And selling CAE tools is a whole different world than selling CAD tools, Smith said. Therein lies Avant!'s main barrier to success with Jupiter, he said.

Changing an entire tool flow is a daunting task for any OEM. Thus some OEMs may choose to use more open EDA tools for the flexibility of tool choices, in order to leverage existing knowledge and protect productivity of design teams.

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EXHIBIT 74

FOCUS - 56 of 56 DOCUMENTS

May 14, 1990

SECTION: Pg. 41; ISSN: 0192-1541

IAC-ACC-NO: 2568679

LENGTH: 1766 words

HEADLINE: Hot design combo

BODY:

By RAY WEISS

Goaded by increasing hardware densities and shortened production schedules, engineers are fast abandoning gate-level design.Coming on strong is the heady combination of program-like descriptions through hardware-descriptions languages (HDLs) and logic-synthesistools, which convert these descriptions to lower-level structural designs. Major computer and microprocessor design houses such as IBM, Sun Microsystems, Data General, Motorola and Stardent have already embraced this technology. Newer companies, such as S3 Inc., which just unveiled its advanced PC chip set (see May 7, page 1), are using its advantages to hit the ground running with leading-edge products.

"VHDLand logic synthesis gave us a competitive advantage," said Dado Banatao, president of startup S3. "VHDL helped our schedule a lot. We could describe the design and simulate it quickly, which let us get the design right early on."

Another major advantage S3 found for HDL/synthesis was its prototyping capability and portability. "Our engineers love it," said Banatao. "You can iterate a design, trying multiple paths, and then feel good about the final design. You know that you explored the design and weren't just stuck with the first implementation."

Synthesis saved the day for S3 when the company had to shift foundries. "It would have taken three months the old way; with VHDL and synthesis it was easy."

High productivity

HDL-driven synthesis promisesan escape from the low-productivity "gate pushing" methods that can't support the complex designs of the 1990s. "HDLs, like VHDL, coupledwith synthesis, enable designers to deal with 500,000-or even 1 million-gate designs," explained David Coelho, vice president of development at Vantage Analysis Inc. "They can do a topdown, multilevel design, simulating at each step to verify the design. They can put more effort at the design front end to ensure that the design is right."

"There's no question that HDLs and logic synthesis will form the basis of ASIC design for the 1990s," said industry analyst Andy Rappaport ofthe Technology Research Group Inc. (Boston, Mass.). "It's happening now, and its going to get very chilly out there for engineers who can't adapt."

Higher productivity and easier design management has sold Matrox Electronic Systems Ltd. (Montreal, Canada) on the HDL/synthesis combination. Using the Verilog HDL and Synopsys synthesis tool, Matrox now has a nine-month turnaround, from initial design to working silicon, for designs with 20,000 to 25,000 gates.

"That's not bad," said Alain Legault, group director of the Matrox Video Graphics Division. "A few years ago, it took us the same time to turn out 8k arrays with schematic capture. And with an HDL, it's much easier to modify a de-

sign to meet changing market conditions during the design phase. A 20k gate design can have 200 to 250 schematic sheets -- a stack over two inches high. Now I can make a VHDL change in a design in two or three days that would have taken four to five weeks with a schematic-capture system."

Magic combination

The magic combination of HDL and logic synthesis gives engineers the key to large-scale, fast design. Heading this revolution are the Verilog and new VHDL hardware-description languages. Verilog, the leading HDL with more than 2,000 licenses and 10,000 users, is being turned, of late, from a proprietary product to a public standard by Cadence Design Systems, its vendor. Moving into prominence is VHDL, the DOD-sponsored, IEEE-standard HDL, which is now supported by most major EDA vendors.

Synthesis the key

But thekey enabling technology is logic synthesis--the emerging commercial technology of converting HDL descriptions into gate implementations directed by user constraints, such as speed and time. Logic synthesis differs from silicon compilation in the level of design detail its tools produce: silicon-compilation tools create a physical design from an input list of design parameters.

Logic synthesis stops at the netlist level, retaining the traditional separation between designer and foundry. To many, this might cause difficulties, since optimized designs must be integrated with layout, a central theme of the older and less successful silicon compilation. Stopping at the netlist means that the silicon foundry must do placement and layout for the ASICs andpost-layout results can affect the design. Moreover, layout-related changes, such as hand routing to minimize critical timing problems, may not be updated to the higher-level models.

Currently, logic synthesis is far from perfect--it's not a pushbutton affair. Logic must be partitioned into synthesizable blocks made with allowable constructs.But it delivers two critical gains: mapping and optimizing designs into ASIC libraries, and a conversion mechanism transforming language constructs into gate-level logic. These free engineers from the drudgery of gate-level implementation.

Out of the gates

"Gate level designis a lot like 'machine language' coding," saud Vantage's Coelho. "The user is caught up in implementation details, not the overall design. The only way to increase ASIC productivity is to move up the abstraction ladder with an HDL/synthesis combination, relieving engineers of fidding with gate details."

And a large number of designers and design managers agree. HDL-based design is used at a large number of companies. IBM, for example, has been using various HDLs and synthesis for years. And Motorola used Verilog and logic synthesis to develop the new 68040, going from prototype breadboarding to a full EDA development approach.

Stardent turned over its next-generation visualizationdesign in nine months--thanks to the Verilog HDL and Synopsys logic synthesis. "The key is that you build a high-level model of your design," said Glen Miranker, Stardent's vice president of engineering. "And you see it as an executable spec, building lower-level models downto implementation."

HDLs and logic synthesis are setting a new levelof design, raising engineers from the gate-level to RTL or higher levels of abstraction. "There's more to this than just logic synthesis and an HDL," said Simon Napper, marketing director for LSI Logic Corp(Milpitas, Calif.), one of the leading ASIC vendors.

"We're enteringa new design era, one that gets engineers out of the low-level implementation business to where engineers can concentrate on higher leveldesign. The design culture is changing from gate-level to a pro manychoices in a language like Verilog," said Sun's Stoddard. "And sometimes the most efficient choices for simulation turn out to perform badly in real logic, or best implementations may compile and simulate slowly."

"In an HDL/synthesis combination, there are dozens of optionsand different approaches," he continued. "It's really an education problem: We have to train engineers to use the most useful subsets andto design efficiently with an HDL. Without that, there is a lot of fumbling around and a lot of wasted effort trying to find the right design/simulation combinations. There is no question that we've made big gains with VHDL and synthesis, but they haven't been as big as we wished."

Motorola's Van Shahan, group leader of the 68040 architectural design team, pointed out some other problems with synthesis. "For one thing, synthesis to the net-list level still leaves the layout problem," he said.

And for large-scale, high-performance merchant parts like the 68040, layout is a key problem. "You have to understand thatchip vendors like Motorola demand a lot more from their silicon thando end users developing their own ASICs," noted Shahan. "They lose 30 to 50 percent of the silicon potential through the tools and foundries. We demand more, because that's what differentiates our processors from what engineers can do with standard ASIC tools."

"We used our own synthesis tools, taken and modified from the Berkeley tool set," he noted. "And the problem is that most synthesis goes to the net-list level. Any changes downstream in the layout (to eliminate timing problems) don't automatically flow back into the high-level descriptions. And you end up with multiple levels of incompatible descriptions or models."

Sun's Stoddard agreed. "Layout problems don't automatically get reflected back in the higher level models. Most chips require some hand tweaking to eliminate timing problems," he said. "Change onething and it affects others--sometimes we get a cascade effect that makes layout and design a nightmare. We need mechanisms to tie all the tools together for both forward development and backward annotation."

Stoddard also noted that a very-high-level behaviroal model was needed to verify designs. "And Verilog and VHDL were too complicated and too close to the final design," he said. "So Sun designers ended upwriting C behavioral models to verify their designs."

Finally, delaying VHDL-based development is a shortage of VHDL chip models. Model vendors, such as Logic Automation and Quadtree, and foundries are building the needed VHDL models. Cadence Design Systems has taken a shortcut--its new VHDL simulator uses the Verilog internal form. Users can mix and match Verilog models with their VHDL designs. Also addressing the problem are Vantage Analyses Systems, with its Spread-sheet, and Mentor, with its new QuickSim 11 simulators, which support mixed-model simulation.

The next level

Chuck Rose, pioneer developer of the early N.2 HDL and now vice president of strategic planning and development at Zycad (Palo Alto, Calif.), doesn't see EDA stopping with today's HDLs–Verilog and VHDL. "Those languages are adequate for most of today's designs, but by the mid-'90s we should see new system tools," he explained. "We need to go up a level higher than today's limited behavioral and RTL levels. I expect we'll see something even resembling the old standby ISP."

And Andy Rappaport concurred. "HDLs are not stopping. There is a lot more to do. I expect VHDL and Verilog to merge by the mid-1990s and move on to other issues, like verifiable designs and even more highly abstract design levels."

The current HDLs support structural (gate level), RTL (operations between fixed elements such as registers and ALUs), and behavioral (programming IF/THEN, WHILE... constructs for state-machine definition) synthesis.

What they don't support is higher level models of engineering constructs, such as pipelines and instruction-set definitions (large-scale state machines, not in an IF/THEN)form). That support will come with the nextgeneration.

LANGUAGE: ENGLISH

IAC-CREATE-DATE: July 27, 1990

LOAD-DATE: November 25, 1996

EXHIBIT

75

FOCUS - 51 of 56 DOCUMENTS

Electronic News

July 1, 1991

SECTION: Pg. 19; ISSN: 0013-4937

IAC-ACC-NO: 3217269

LENGTH: 79 words

HEADLINE: CAE SOFTWARE: Gould ...

THIS IS THE FULL TEXT

BODY:

Gould AMI is developing gate array and standard cell libraries for use with Synopsys' Design Compiler software The libraries, set for availability in the third quarter, are to contain some 150 functions. In addition, Gould is also to develop software to allow the Synopsis libraries to support EDIF translators from most major CAE vendors, toallow output of its cells from the Synopsis synthesis tools to work with various schematic capture and logic simulation pack ages.

LANGUAGE: ENGLISH

IAC-CREATE-DATE: July 16, 1991

LOAD-DATE: November 25, 1996

EXHIBIT 76

3 of 14 DOCUMENTS

Business Wire

April 8, 1996, Monday

DISTRIBUTION: Business Editors & Computer Writers

LENGTH: 785 words

HEADLINE: Synopsys' VHDL System Simulator Fully Compliant With VITAL '95 ASIC Library Standard; VITAL support expanded by Synopsys' VITAL '95 library generator

DATELINE: MOUNTAIN VIEW, Calif.

BODY:

April 8, 1996-- Synopsys, Inc. (NASDAQ:SNPS) today announced that version 3.4b-Vital of its VHDL System Simulator (VSS) offers 100 percent compliance to the VITAL '95 (VHDL Initiative Toward ASIC Libraries) specification stipulated in IEEE 1076.4.

VSS 3.4b-Vital also provides simulation acceleration of VITAL '95 libraries. In addition, Synopsys' Library Compiler automatically generates VITAL '95 libraries from Synopsys synthesis libraries.

"We enthusiastically support the VITAL '95 standard, and believe that its ratification establishes an important milestone toward the proliferation of VHDL ASIC libraries," said Emil Girczyc, general manager of Synopsys' design verification business unit. "This announcement represents the results of a three-year collaboration with our ASIC vendor partners to provide VHDL sign-off capability to our mutual customers."

Synopsys' Semiconductor Vendor Program (SVP) partners have already begun using VSS 3.4b-Vital (beta version) to qualify their libraries for sign-off. "AMI was pleased to be part of a select beta team to test Synopsys' new VITAL '95-compliant simulator," said Steve Wadsworth, AMI senior staff software engineer. "Our rigorous testing has shown us that Synopsys is committed to providing a quality simulation product that adheres to the VITAL '95 standard. Our VITAL '95-compliant libraries will be available in conjunction with Synopsys' production software release."

"We are very pleased with Synopsys' support of the VITAL standard," said Sarita Thakar, Design Integrator VHDL Staff Engineer, DA Systems Development, ASIC Core Technology Group, VLSI Technology Inc. "Our experience testing VSS with our VITAL libraries shows that VSS fully conforms to the VITAL '95 standard."

"We see portability between simulators as an important benefit of conformance to VITAL '95," added Tom VandenBerge, Manager DA Systems Development, ASIC Core Technology Group, VLSI Technology Inc. "With Synopsys' support of industry standards, it's a win-win-win scenario that allows us to deliver capabilities to our mutual customers faster. When EDA and ASIC vendors combine their respective talents, the customer always wins."

Synopsys was the first to provide ASIC sign-off in VHDL with the introduction of its FTGS (full-timing gate simulation) modeling methodology over two years ago. The company has continued to play a key role in the development and adoption of VHDL sign-off capabilities as an active participant in the VITAL technical committee.

Support for the VITAL '95 standard provided by VSS 3.4b-Vital includes full compliance and acceleration. VSS 3.4b-Vital also carries forward the sign-off capabilities established in the FTGS engine to provide ongoing support of the stringent requirements set by many of Synopsys' ASIC vendor partners. The VSS VITAL implementation delivers up to 3x improvement in capacity and 30 percent improvement in speed over the FTGS engine in version 3.3b. In addition, VSS 3.4b has been enhanced to provide performance increases of up to 70 percent at the register transfer level and the behavioral level over the 3.3b release.

Synopsys' 3.4a software release enables users to generate VITAL '95-compliant libraries. The library generator in version 3.4a of Synopsys' Library Compiler can automatically generate VITAL '95-compliant libraries in addition to other models.

Price and Availability

VSS 3.4b-Vital with VITAL '95 support will be available in May '96, with pricing set at $ 24,000 U.S. list. Existing VSS Expert customers will receive VSS 3.4b-Vital as a free upgrade.

Library Compiler 3.4a, for generation of VITAL '95 libraries, is available now, with pricing set at $ 25,000 U.S. list.

Synopsys, Inc. (NASDAQ:SNPS) develops, markets and supports high-level design automation models and software for designers of integrated circuits (ICs) and electronic systems. The company pioneered the commercial development of synthesis technology, which serves as the foundation of the company's high-level design methodology. Synopsys offers a comprehensive set of synthesis, simulation, test, and design reuse solutions, which support both Verilog HDL and VHDL. -0-

Note to Editors: Synopsys is a registered trademark of Synopsys Inc. VSS, VSS Expert and Library Compiler are trademarks of Synopsys Inc. Verilog is a trademark of OVI.

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LOAD-DATE: April 9, 1996

13 of 15 DOCUMENTS

Electronic Engineering Times

July 26, 1999

LENGTH: 1222 words

HEADLINE: Synopsys tips next spin on synthesis

BYLINE: Richard Goering

BODY:

MOUNTAIN VIEW, CALIF. - A new generation of logic-synthesis technology that promises tight integration with placement is nearing product release at Synopsys Inc., and is currently in use at four partner companies. But Synopsys may be heading for a legal squabble with Cadence Design Systems Inc. over use of the Library Exchange Format (LEF), which will be important to the new product's success.

Synopsys' so-called "unified synthesis and placement technology," slated for a fourth-quarter rollout, is apparently the basis of PhysOpt, an unannounced tool the company demonstrated privately at the recent Design Automation Conference in New Orleans. PhysOpt got generally good reviews in a recent mailing of the E-Mail Synopsys User's Group (ESNUG).

The tool will go head to head with the Cadence Envisia PKS synthesis tool (see July 12, page 1) and, like PKS, will feature concurrent optimization between synthesis and placement. It's also Synopsys' answer to startups MagmaDesign Automation and Monterey Design Systems, both of which are promising integrated physical-design systems with some synthesis features.

Disclosure of the Synopsys plan comes as Cadence reported a downturn in last week's quarterlies, which signals an intensifying battle between the two companies for leadership in the electronic-design-automation arena (see related story, page 1).

The new technology goes well beyond Synopsys' Chip Architect, announced in February. Where Chip Architect basically wraps floor planning and placement around the existing Design Compiler product, the new tool fundamentally changes synthesis. Unlike Chip Architect, which focuses on chip-level integration, the new synthesis technology is aimed at the toughest, most performance-critical individual blocks.

In a private briefing last week, Synopsys executives disclosed that the new technology is in use at Matrox, NEC, NVidia and STMicroelectronics. Synopsys representatives showed impressive, but unattributed, benchmark results and outlined the scheme's purported advantages over Cadence's Envisia PKS.

But Synopsys declined details about the inner workings of the tool or even the name it will carry. Sanjiv Kaul, vice president and general manager of Synopsys' physical synthesis unit, called "PhysOpt" an "internal code name" that will likely not be the final product name.

Kaul also said Synopsys intends to eventually field a complete physical- design solution, including cell-level routing, which will not be provided in the impending synthesis-and-placement rollout. "We intend to go all the way to GDSII," he said, "because that's how silicon is built."

Unified synthesis and placement, Kaul said, is "one product" based on years of research at Synopsys. "We are not taking a standard synthesis product and a placement product and tying them together. This is a fundamentally new synthesis tool," he said.

But a key to the tool's success is LEF, a format Cadence currently owns even though its status is changing. Both the new Synopsys synthesis tool and Chip Architect need physical IC libraries, many of which are in LEF.

Kaul said Synopsys can use LEF today because of the Federal Trade Commission's scrutiny of Cadence's 1997 acquisition of Cooper & Chyan Technologies. "One thing the FTC did was give permission to use standard formats," said Kaul.

Not so, replied Shane Robison, vice president of the design productivity group at Cadence (San Jose, Calif.). "Synopsys is making the assumption we won't defend that intellectual property. They may be surprised," Robison said.

Robison said Cadence has offered LEF to Synopsys under its Connections program, but Synopsys has refused. Currently, Cadence is negotiating with the Silicon Integration Initiative to take over LEF, in which case it would presumably be usable by anyone (see June 28, page 4). But whether Cadence goes after Synopsys for allegedly jumping the gun on LEF remains to be seen.

Good results

Though Synopsys has provided few details about its new technology, two designers contacted by EE Times gave it good reviews. "Mainly what we're seeing is that we're able to achieve target performance and area an order of magnitude faster with much less effort," said Jean-Jacques Ostiguy, vice president of engineering at Matrox Corp. (Montreal).

Ostiguy hasn't used the new technology in production, but ran test cases on large graphic-chip designs. His benchmarks focused on reducing iterations and improving speed, not boosting performance, but he said there was a "slight" performance increase. He also said the technology produced a "final quality placement" that was turned directly over to Cadence tools for routing.

Chris Malachowsky, vice president of engineering at NVidia Corp. (Santa Clara, Calif.), also ran test cases focusing on turnaround time. He said the new Synopsys technology was able to meet target timing and routability for two difficult blocks in a single day, compared with a few weeks using NVidia's previous design flow. "It looks like it's a great start and it's producing good results," he said.

The Synopsys technology potentially shifts the ASIC handoff model, and NEC Corp. is working with Synopsys on a new approach, said Hiroshi Sakuma, department manager for NEC's System LSI Engineering Division. Sakuma said NEC will accept either a register-transfer-level handoff or a fully placed net- list. "In both of the cases, our intention is to use the Synopsys placement as the final one and to do only routing," he said.

In the ESNUG postings, one anonymous engineer said that PhysOpt "is just a few more lines in your DC Design Compiler script. No need to buy or learn Chip Architect. More importantly, no more bloody wire-load models!"

Another posting noted that PhysOpt doesn't do clock-tree synthesis, meaning that final placement will have to be redone. Synopsys' Kaul declined to comment on any of the ESNUG reports.

Kaul was, however, willing to talk about how the new Synopsys technology compares with Cadence's Envisia PKS. He claimed that PKS doesn't start incremental placement and optimization until key synthesis decisions have already been made; that its use of Cadence's QPlace product introduces a second timing engine; and that it doesn't produce a final placement.

But Michael Carrell, Cadence's Envisia PKS product manager, said that most of the tool's structuring and mapping occurs with placement; that it has only one timing engine; and that it can produce a "legal and routable" placement.

Brent Gregory, a fellow at Synopsys, stressed the importance of integrating placement with register-transfer-level synthesis rather than gate-level optimization. "A lot of architectural decisions are made at the RTL that cannot be undone at the gate level," he said.

Synopsys will argue that physical-design tools from Sapphire, Silicon Perspective, Magma, Monterey and Avant! start placement and optimization too late.

In a benchmark with an unidentified customer, Synopsys claims to have taken a design that took three months to complete with a worst-case negative slack of -1.5 ns, and redone it in a single day while reducing the negative slack to -0.86 ns.

The ESNUG mailings are hosted at www.deepchip.com.

-Additional reporting by Yoshiko Hara.

LOAD-DATE: July 24, 1999

FOCUS - 38 of 56 DOCUMENTS

Business Wire

February 8, 1999, Monday

DISTRIBUTION: Business Editors/Technology Writers

LENGTH: 977 words

HEADLINE: American Microsystems Signs Off On Synopsys' VCS; Provides VCS Sign-off Support for AMI's 0.35-micron ASIC Process

DATELINE: MOUNTAIN VIEW, Calif.

BODY:

--(BUSINESS WIRE)--Feb. 8, 1999--SynopsysInc. (Nasdaq:SNPS), the design technology leader for complex IC design, today announced that American Microsystems, Inc. (AMI) will provide certified sign-off support for Synopsys' VCS(TM) Verilog simulator. AMI is targeting its gate-array and standard-cell digital CMOS ASIC products in 0.35-micron process technology. "By delivering VCS sign-off support, AMI is enabling a seamless development path for deep submicron ASIC designs," said Bob Smith, AMI's director of design technology. "VCS provides the accuracy and verification performance that our customers require for their complex ASIC designs. Using AMI's EDA Library and Integrated Tool Environment (ELITE), designers can verify their Verilog RTL designs using VCS, synthesize using Synopsys' Design Compiler(TM), and simulate gate-level designs with VCS for rapid, sign-off quality results. "VCS has always set the standard for Verilog simulation speed and capacity and now it's setting the standard for ASIC sign-off libraries," said Steve Smith, director of marketing for the simulation technology group at Synopsys. "With the addition of AMI's support, our mutual customers can be assured that VCS offers the best simulation sign-off capability available." AMI's new 0.35-micron CMOS ASIC process provides advanced digital design capabilities targeting applications in the telecom access switching, mobile communications, industrial controllers, data networking, and computer/peripheral markets. Its high-density characteristics allows up to 27,000 gates/mm2, giving designers the flexibility to shrink die sizes or double the number of gates on a die of the same size compared with their earlier 0.5-micron process. The process is optimized at 3.3 volts for low power operation. VCS is the industry's highest performance and fastest-growing Verilog simulator. It's built upon proven native compiled technology and incorporates Radiant optimizations and RoadRunner(TM) cycle-based technology for extremely fast simulation, without requiring any methodology changes. This combination makes VCS ideal for all phases of the design cycle. In addition, VCS is supported by over 150 of the most advanced technology libraries currently available from every major semiconductor vendor worldwide and has obtained the Si2 Library Qualification Seal. VCS also offers full support of Open Verilog International and IEEE industry standards and interfaces to leading third-party verification tools and models, including hardware/software co-verification, graphical debug and analysis, code coverage and testbench generation. VCS is part of Synopsys' powerful, suite of functional verification products and services. Synopsys offers the industry's fastest Verilog and VHDL simulators, a comprehensive range of proven IP models for simulation, the innovative Eagle(TM) hardware/software co-verification tools, and the VERA(TM) testbench automation and analysis products to help meet the challenges of functional verification of complex designs. Synopsys complements this suite with a unique static verification offering, which includes formal verification, static timing analysis and automatic test pattern generation. These tools conform to industry standards to ensure easy integration with customer design environments. Sign-off support for VCS for AMI's 0.35-micron digital CMOS process technology is available immediately.

About American Microsystems, Inc.

American Microsystems Inc., headquartered in Pocatello, Idaho, pioneered the development of application specific integrated circuits (ASICs) in 1966. Over the last 33 years, AMI has remained a leading ASIC supplier for communication and industrial applications. AMI is committed to providing the best total solution employing the latest digital and

analog capabilities. AMI offers a broad range of analog and mixed-signal ASICs, ASIC translation services, mixed-signal application-specific standard products (ASSPs), and CMOS foundry services with unprecedented design-to-production span times. AMI is ISO 9001 certified. For more information on AMI's capabilities, write to American Microsystems Inc., 2300 Buckskin Road, Pocatello, Idaho 83201, or call (208) 233-4690. Visit the AMI home page at www.amis.com.

About Synopsys

Synopsys Inc. (Nasdaq:SNPS), is a leading supplier of electronic design automation (EDA) solutions to the global electronics market. The company provides comprehensive design technologies to creators of advanced integrated circuits, electronic systems, and systems on a chip. Synopsys also provides consulting services and support to its customers to streamline the overall design process and accelerate time-to-market. Additional information about Synopsys is available at http://www.synopsys.com. Synopsys is a registered trademark, VCS and Design Compiler are trademarks of Synopsys Inc. All other trademarks or registered trademarks mentioned in this release are the intellectual property of their respective owners.

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LOAD-DATE: February 9, 1999

FOCUS - 4 of 56 DOCUMENTS

Business Wire

October 2, 2000

SECTION: Pg. 2524

IAC-ACC-NO: 65634945

LENGTH: 979 words

HEADLINE: Synopsys Advances DFT Closure With Integration of Testability in the Physical Domain and Expansion of ATPG Capabilities.

AUTHOR-ABSTRACT:
THIS IS THE FULL TEXT: COPYRIGHT 2000 Business Wire

BODY:

Business/Technology Editors

MOUNTAIN VIEW, Calif.--(BUSINESS WIRE)--Oct. 2, 2000

DFT Compiler Integration with Physical Compiler and TetraMAX ATPG's

New Advanced Sequential Technology Enable Designers to Achieve

Significantly Faster DFT Closure

Synopsys, Inc. (Nasdaq:SNPS), today announced new capabilities that facilitate design-for-test (DFT) closure by integrating its DFT Compiler(TM) product within the company's Physical Compiler environment, enabling fast timing closure with fully testable semiconductor designs. In addition, Synopsys announced it is rolling out next-generation sequential automatic test pattern generation (ATPG) technology in its TetraMAX(TM) ATPG tool. These capabilities give designers new advantages in their battle to achieve DFT closure and provide the increased pattern generation power that DFT engineers need to test today's complex systems-on-chip.

Physical Domain Integration With Test

As the design community moves to adopt physical synthesis flows, it is evident that testability must be taken into account at all stages of the design process to achieve rapid and predictable DFT closure. DFT closure is the ability to meet all mandated DFT requirements at every phase of the SoC design flow. The biggest challenges to attaining DFT closure in physical synthesis flows come in two areas-timing on the scan paths and routing congestion due to scan wiring.

With the integration of DFT Compiler in the Physical Compiler environment, Synopsys is providing a significant new capability to optimize scan DFT without cumbersome scripts and data transfers. DFT Compiler uses placement information and employs a constraint-driven scan-ordering algorithm to optimize scan chains within the physical synthesis environment. The tight integration of scan ordering and physical synthesis avoids the risks of routing congestion and timing violations that may arise from DFT without physical information. By addressing scan ordering within the unified test synthesis and placement flow, Synopsys' benchmarks show routing congestion can be reduced by an average of 10 to 15 percent with noticeable improvements in overall timing. Finally, this capability further improves the automatic flow between DFT Compiler and TetraMAX ATPG by completely eliminating the need for reformatting ATPG vectors.

According to David Chiappini, physical design team leader, Matrox Graphics Incorporated, "We strongly believe that the integration of physical scan ordering in Synopsys' unified DFT and physical synthesis design methodology will allow Matrox to achieve timing closure more rapidly and predictably."

New TetraMAX with Sequential ATPG Technology

Synopsys has enhanced its TetraMAX ATPG tool with advanced sequential pattern generation technology. The new sequential ATPG engine plugs into TetraMAX's multi-technology architecture, and enables designers to reach their manufacturing fault coverage goals for a broader range of circuits, including near-full scan designs with non-optimal testability. As ease of use was a key development goal, this new capability is completely automatic-designers will be able to reach their test manufacturing program requirements without additional setups or output modifications. For example, in some large designs, quickly achieving timing closure and optimal scan chain ordering may require removing elements from the scan chain. This reduces the testability typically needed for high-test coverage. In such cases, TetraMAX can transparently invoke the advanced sequential engine's extra ATPG power to compensate for the reduced testability-resulting in uncompromised device quality and defect levels while enabling much faster time-to-market.

"Our customers have been keenly interested in our efforts to provide powerful test technology in order for them to meet ever more stringent manufacturing quality requirements. In response, we've continued to add state-of-the-art technology into our DFT Compiler and TetraMAX ATPG tools," said Antun Domic, vice president and general manager of Synopsys' Nanometer Test and Analysis Group. "These technologies provide key improvements in our DFT closure flow working in conjunction with Synopsys' Physical Synthesis technology."

Pricing and Availability

DFT Compiler 2000.11 and TetraMAX ATPG 2000.11 begin shipping in December 2000. Current customers will receive these enhancements at no additional charge as a maintenance upgrade. Pricing for DFT Compiler is $ 15,000, and pricing for TetraMAX ATPG is $ 33,500 for one-year technology subscription licenses (TSLs).

Synopsys' Versatile Test Solution

Synopsys is the leading supplier of IC test automation solutions, offering a complete line of integrated test products and services. Synopsys' test offering includes DFT Compiler for 1-Pass test synthesis, BSD Compiler for IEEE 1149.1 (boundary scan) support and TetraMAX ATPG for test pattern generation. These products enable design teams to efficiently meet their DFT closure goals within Synopsys' industry-leading synthesis design flows.

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS), headquartered in Mountain View, California, creates leading electronic design automation (EDA) tools for the global electronics market. The company delivers advanced design technologies and solutions to developers of complex integrated circuits, electronic systems and systems on a chip. Synopsys also provides consulting and support services to simplify the overall IC design process and accelerate time to market for its customers. Visit Synopsys at http://www.synopsys.com.

IAC-CREATE-DATE: October 2, 2000

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FOCUS - 1 of 56 DOCUMENTS

Business Wire

June 6, 2001

SECTION: Pg. 0391

IAC-ACC-NO: 75317567

LENGTH: 586 words

HEADLINE: Synopsys Delivers New Versions of FPGA Compiler II and FPGA Express to Enhance Productivity for Complex Designs.

AUTHOR-ABSTRACT:
THIS IS THE FULL TEXT: COPYRIGHT 2001 Business Wire

BODY:

Business Editors/High-Tech Writers

MOUNTAIN VIEW, Calif.--(BUSINESS WIRE)--June 6, 2001

Synopsys Inc. (Nasdaq:SNPS), the technology leader for complex IC design, today announced new versions of its FPGA synthesis solution: FPGA Compiler II(TM) and FPGA Express(TM). In this latest release, version 3.6, Synopsys delivers several enhancements that make FPGA design easier and more efficient than ever before.

"More and more of our customers are using FPGAs for sophisticated applications," said Aart de Geus, chairman and CEO of Synopsys. "They need robust, ASIC-like design tools. We have been steadily increasing our investment in such FPGA design solutions to meet their growing needs."

Popular Solutions

Synopsys' FPGA Synthesis solution is in broad use today. FPGA Express is available through OEM channels and is accessed by over ten thousand designers around the world. FPGA Compiler II, which includes advanced capabilities such as full retiming, is sold directly by Synopsys and is used at over 700 customer sites around the world.

"We used FPGA Compiler II successfully on our latest design," said Mark Halvorsen, product development manager at Inari Inc. "We estimate that Synopsys tools and flows saved us at least two months and were critical to meeting our time-to-market goals."

Carle Banville, a hardware design manager at Matrox, recently purchased FPGA Compiler II. He commented, "We're able to buy a full line of design products from Synopsys. Not having to mix and match makes my job much easier."

Easy Access and New Capabilities with Version 3.6

Synopsys FPGA Compiler II supports all devices from Altera (Nasdaq:ALTR) and Xilinx (Nasdaq:XLNX). Version 3.6 now contains algorithms to support future device and software offerings from these leading silicon vendors. These algorithms are activated by downloading plug-in modules, which will be made available by Synopsys to customers who have registered on the Synopsys FPGA Compiler II web page.

FPGA Express and FPGA Compiler II both feature a new intuitive graphic user interface to select the I/O buffers for Xilinx Virtex-II devices. This significantly reduces the effort needed to design for these high-end devices by streamlining the HDL source code as well as preventing invalid combinations of I/O standards, slew rate and drive strength. In

addition, version 3.6 delivers specialized high-performance multiplier support and a critical path browser, making FPGA Express and FPGA Compiler II even easier to use for designing high-performance FPGA devices.

For more information about Synopsys' FPGA synthesis solution, visit http://www.synopsys.com/fpga or see us in booth no. 2400 at DAC 2001, June 18-21 in Las Vegas.

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS), headquartered in Mountain View, California, creates leading electronic design automation (EDA) tools for the global electronics market. The company delivers advanced design technologies and solutions to developers of complex integrated circuits, electronic systems, and systems on a chip. Synopsys also provides consulting and support services to simplify the overall IC design process and accelerate time to market for its customers. Visit Synopsys at http://www.synopsys.com.

IAC-CREATE-DATE: June 6, 2001

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FOCUS - 27 of 56 DOCUMENTS

Business Wire

November 10, 1999

SECTION: Pg. 0345

IAC-ACC-NO: 57481020

LENGTH: 1363 words

HEADLINE: Synopsys' New Physical Compiler Solves the Timing Closure Challenge Using Unrivaled PhysOpt Engine.

AUTHOR-ABSTRACT:
THIS IS THE FULL TEXT: COPYRIGHT 1999 Business Wire

BODY:

MOUNTAIN VIEW, Calif.--(BUSINESS WIRE)--Nov. 10, 1999--

High Performance Graphics Chips Successfully Tape Out

with Physical Compiler

Synopsys Inc. (Nasdaq:SNPS), the technology leader for complex IC design, today unveiled Physical Compiler, a fundamentally new integrated circuit (IC) design tool that unifies synthesis and placement into a single product. Physical Compiler's innovative RTL-to-placed-gates capability results in the fastest path to timing closure, together with the highest circuit performance for today's most complex designs. Advance access to Physical Compiler allowed Matrox Electronic Systems Ltd. and NVIDIA Corporation to tape out their next-generation graphics chips weeks ahead of schedule. Physical Compiler is key to Synopsys' physical synthesis solution, which also includes Chip Architect, introduced in January 1999 and FlexRoute, released in May 1999.

"Synopsys has devoted tremendous effort to solving the timing closure challenge beginning several years ago when designers identified it as their single largest obstacle in the implementation flow," said Aart de Geus, chairman and chief executive officer of Synopsys. "Now, with Physical Compiler, RTL designers will output placement to meet their timing objectives. By unifying synthesis and placement, this tool is causing a fundamental change in the design landscape, which will result in final placement moving to the front end of IC design."

"Physical Compiler allowed us to tape out our latest graphics chip four weeks ahead of our schedule. In our competitive market, four weeks may prove to be the difference between having a competitive product or missing the market window all together," said Jean-Jacques Ostiguy, vice president, graphics ASIC with Matrox Electronic Systems Ltd., Montreal, Canada. "Physical Compiler exceeded our expectations and plugged right into our flow. It gave us predictabl and outstanding results. To date, we have upgraded over 50 percent of our Design Compiler licenses to Physical Compiler and are installing the tool across all of our design centers."

"We recently taped out our future generation GeFORCE chip using Physical Compiler. Through the use of it, we were able to compress our back end schedule by three to four weeks," said Chris Malachowsky, vice president of engineering with NVIDIA Corporation, Santa Clara, CA. "The results are stunning -- by utilizing Physical Compiler, we were able to achieve timing with minimal iterations. In days, we exceeded the results that previously took dozens of post-placement and post-route iterations over multiple weeks to achieve. Physical Compiler is now considered a critical component of our design flow."

"For advanced System LSI designs in our current 0.18-micron and our next generation 0.13-micron technologies, timing problems require a new hand-off model," said Yoshitada Fujinami, chief manager, System LSI Design Engineering Division, NEC Corporation, Tokyo, Japan. "Our extensive evaluation has shown that Physical Compiler has the capability to produce, in a single run, better timing after routing and less congestion than we were able to accomplish within weeks using conventional techniques. We are on track to include Physical Compiler in our OpenCAD(R) design kit in Q2 2000."

Features and Benefits

With Synopsys' Physical Compiler's RTL-to-placed-gates capability, users achieve the shortest path to post-route timing closure and the best circuit performance. For example, on one customer design, the best circuit clock rate achieved--after more than six months of traditional design iterations--was 155 MHz. On the same customer design, Synopsys' Physical Compiler produced circuit performance exceeding 180 MHz, in less than one day.

Physical Compiler is built on Synopsys' unified logical and physical database. In addition to Synopsys' world class synthesis technology, it incorporates the patent pending FlexPlace placement technology and proprietary congestion minimization algorithms. At the heart of the tool is the PhysOpt engine, which unifies these technologies and simultaneously optimizes for all the design cost functions.

Synopsys' Physical Compiler offers users the following features: -0-

-- RTL-to-placed-gates capability that unifies synthesis and placement, eliminating the need for wire load models and iterations between logical and physical design
-- A common database, user model, constraints, timer and libraries allowing easy adoption for existing Synopsys Design Compiler users, resulting in minimal adoption costs and learning curve
-- Interfaces to industry-standard routers that allow the tool to easily plug into any current design methodology. The resulting netlist and placement work seamlessly in production flows with routers such as Cadence's Silicon Ensemble and Avant!'s Apollo
-- Accurate global routing technology and innovative congestion optimization algorithms that result in a close correlation between Physical Compiler and post-final-route results
-- Test, power, datapath and DesignWare optimization solutions are automatically addressed due to the tool's seamless integration with other Synopsys synthesis solutions

-0-

Physical Synthesis Solution

Physical synthesis promises to become the IC design community's most effective design flow. Pioneered by Synopsys, this flow helps designers rapidly complete today's complex 0.18-micron and below system-on-a-chip (SoC) designs. Synopsys' physical synthesis is the only method that completely ties both physical and logical design together in a manner that enables chip-level timing closure on highly complex ICs. The overall design flow includes the new Chip Architect(TM) design planner and the FlexRoute top-level router and leverages industry-standard tools like Design Compiler(TM), Module Compiler(TM) and PrimeTime(R). Today's release of Physical Compiler further demonstrates Synopsys' objective of helping customers solve one of their most difficult design challenges: that of achieving timing closure.

"Synopsys' Physical Synthesis flow, which includes Chip Architect and Physical Compiler, is proving to be critical to enable us to achieve timing closure quickly and predictably," said Jean-Pierre Geronimi, CAD director, Central R&D, STMicroelectronics, Crolles, France. "In over ten designs we have run with Physical Compiler, we have been impressed with the outstanding quality of results and the tool's stability and ease with which it plugs into the rest of our flow. We anticipate having our first tape out with Physical Compiler before the end of the year and a design kit for our customers by Q2 2000. "

With the success that these initial partners and customers have seen, Synopsys is expecting to announce several additional partnerships with semiconductor vendors and customers by the end of 1999.

Pricing and Availability

Synopsys' Physical Compiler perpetual license pricing starts at US $ 300,000. The product is currently shipping in limited availability and will be available for general release in April 2000.

About Synopsys

Synopsys Inc. (Nasdaq: SNPS), is the leading supplier of electronic design automation (EDA) products and services to the global electronic market. The company provides comprehensive design technologies to creators of advanced integrated circuits, electronic systems and systems on a chip. Synopsys also provides consulting services and support to its customers to streamline the overall design process and accelerate time-to-market. Additional information about Synopsys is available at http://www.synopsys.com.

IAC-CREATE-DATE: November 10, 1999

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Electronic Engineering Times

November 15, 1999

LENGTH: 1686 words

HEADLINE: Synthesis takes two giant steps -- Synopsys' long-awaited Physical Compiler unites placement with synthesis

BYLINE: Richard Goering

BODY:

MOUNTAIN VIEW, CALIF. - Promising a dramatic shift in the way high- performance chips are designed, Synopsys Inc. last week rolled out Physical Compiler, which tightly couples synthesis with placement in a single product. Based on long-awaited technology code-named PhysOpt, the product has already received rave reviews from customers, who are claiming huge time savings and performance gains.

But Synopsys' product enters a market already crowded with new chip design solutions, and competitors point out that Physical Compiler lacks detailed routing and other important physical design features. One of Synopsys' newer competitors, startup Magma Design Automation, this week is announcing a contract award and endorsement from Fujitsu.

Behind the competitive posturing is a clear shift to a new generation of design tools that can provide substantial productivity gains. And the inexorable trend toward tying synthesis and layout into a single process is accelerating, exemplified by the full, legal placement provided by Physical Compiler.

"What we are announcing is one of the crown jewels of our work," said Aart de Geus, chairman and chief executive officer of Synopsys. "It brings together fundamental synthesis technology with fundamental placement technology, all in one solution."

The product has already led to successful tapeouts, de Geus said, and has generated significant revenue for Synopsys in the past two quarters. At press conferences last week, designers from Nvidia, Matrox, NEC and STMicroelectronics spoke of slashing weeks off design cycles, while in some cases reducing negative slack by an order of magnitude or more.

For high-performance blocks, Physical Compiler underlies a methodology in which register-transfer level (RTL) designers can go all the way to final placement. That, in turn, promises to change today's EDA landscape.

"Our belief is that this can really change the whole layout market," said de Geus. "We are looking at a significant piece of that market now being connected to front-end design, and of course we won't sit still until we fill in whatever blanks are left."

Synopsys' recent thrust into physical design puts considerable pressure on Cadence Design Systems Inc. and Avanti Corp., although both are responding with solutions of their own. Cadence's Envisia PKS links synthesis and placement into a single product, and Avanti's Jupiter closely ties synthesis to Avanti layout tools.

What no other competitor has, however, is Synopsys' overwhelming market leadership in synthesis. With recent financial results that make it the EDA industry's revenue leader, Synopsys is riding a wave of considerable momentum.

Physical Compiler is a complete synthesis offering used in place of the existing Design Compiler for high-performance blocks. It includes a timing- driven placement capability called FlexPlace. PhysOpt is described as an " engine" that links synthesis, FlexPlace, timing analysis and routing- congestion analysis-the four main components of Physical Compiler.

Starting at $300,000 per seat, Physical Compiler is not for everybody. " Right now it applies to 20 percent of our customer base-the people who really have timing problems today," said de Geus. "But this number will change very rapidly."

Physical Compiler is part of Synopsys' "physical synthesis" road map, which includes Chip Architect, FlexRoute and the PrimeTime static timing analyzer. Chip Architect is a chip-level tool that offers floor planning and placement. It can feed placement data into Physical Compiler, take the block-level output and assemble it into a chip. FlexRoute is a top-level detailed router.

All that Synopsys is missing is detailed cell-level routing. But that, say some competitors, is a significant flaw.

"Physical Compiler cannot guarantee timing closure, routing completion and reliability of the final GDSII layout," said Rajeev Madhavan, chief executive officer of Magma Design Automation. Madhavan said Magma's Blast Fusion has beaten Physical Compiler in customer benchmarks, showing up to 20 percent higher performance.

"The real deep-submicron issues are design-closure issues-signal integrity, power, yield and packaging-not just timing," said Kevin Walsh, vice president at Sapphire Design Automation. Walsh said logic designers "need RTL handoff with predictable timing, including power and signal integrity issues, not the added burden of doing placement."

Sanjiv Kaul, vice president and general manager of Synopsys' physical synthesis business unit, argued that linking synthesis and placement is "the single biggest thing that needs to be done for timing closure." Adding detailed routing would have a minimal effect, he said.

Making a case for the linkage of synthesis and layout, Kaul said front-end timing is unpredictable, given that all nets with the same fanout are assumed to have the same interconnect delay. But that's not true after placement, which can change timing dramatically.

The proof is in the pudding, however, and Synopsys is letting users tell much of the story. That impressed John Cooley, moderator of the E-Mail Synopsys User's Group (ESNUG), who said Synopsys has achieved a "totally different level of credibility" than most other EDA vendors with chip design solutions.

Faster chips, faster designs

Bogdan Staicu, design flow specialist at Matrox Electronic Systems Ltd. (Montreal), spoke of his company's use of Physical Compiler with a 360-MHz 3- D graphics chip. Physical Compiler shaved four weeks off the part's design schedule, simplified the floor planning process and resulted in a chip that's 5 percent faster, Staicu said.

Asked about the product's $300,000 price tag, Staicu replied, "If it allows us to get a product fast to market, it's worth it." He noted, however, that detailed routing would be a welcome addition to the product.

Nvidia Corp. (Santa Clara, Calif.) used Physical Compiler on a 750,000-gate block on a high-performance graphics chip. Chris Malachowsky, Nvidia's vice president of engineering, said the company shaved three to four weeks off the tapeout schedule, saw a 5 to 10 percent improvement in post-layout timing and reduced worst-case negative slack from -8 ns to -0.86 ns in a single run.

"We saved time, picked up a performance boost, and it really did just fly through the Avanti router," Malachowsky said.

Both Staicu and Malachowsky, however, have so far used Physical Compiler only at the gate level.

At NEC, Physical Compiler reduced worst-case negative slack from -15.73 ns to -0.49 ns on one block compared with the previous methodology, which used Design Compiler, said Nobuyuki Nishiguchi, department manager of the system LSI operations.

But Fujitsu's experience with Magma's Blast Fusion shows that Synopsys doesn't necessarily have a monopoly on significant performance gains. Although the dollar amount was not revealed, Fujitsu has agreed to what Magma's Radhavan called a "massive, worldwide deployment" of Blast Fusion, by far Magma's biggest order to date.

Gerry Atterbury, director of advanced intellectual property (IP) methodologies at Fujitsu, said his company ran a number of benchmark designs through Blast Fusion and was able to reach timing closure in all cases with no iterations. "It took roughly 20 percent of the time taken with our previous tools," he said. In addition, area was improved from 5 to 50 percent, and performance from 5 to 30 percent, compared with the previous methodology.

Fujitsu has not looked closely at Physical Compiler, Atterbury said.

Malachowsky said Physical Compiler was very easy to add to Nvidia's existing design flow. That's the claim Synopsys makes as well. But the tool does require some different inputs than Design Compiler. Those include physical libraries and physical constraints, such as the aspect ratios of blocks, input/output locations, obstructions and legal placement areas.

One input format to Physical Compiler is the Library Exchange Format (LEF). Cadence's decision to donate LEF text to the Silicon Integration Initiative (Si2) may put to rest a potential conflict between the EDA leaders over the use of LEF.

Synopsys said it breaks new ground with its FlexPlace placer. The key technologies here include linear wire-length reduction, which directly reduces the total Manhattan wire length; unpartitioned gate placement, so that FlexPlace adjusts every gate's position within its entire placement region; and direct quality measures, such as linear vs. quadratic wire length.

One feature currently missing from Physical Compiler is clock tree synthesis. "Customers are doing clock trees elsewhere, and the flow works now, " said Kaul, "but I think we will eventually add it in."

Synopsys claims a number of advantages for Physical Compiler compared with its most direct competitor, Cadence's Envisia PKS. One is integration with a range of Synopsys technologies in such areas as timing, power and test, as well as the DesignWare library. Another is an ability to work equally well with Cadence or Avanti placement and routing tools.

"We stand by our view that PKS is not much more than what we call Floorplan Manager," said Kaul. "It's built on two different infrastructures."

But Paul Estrada, corporate vice president for IC implementation at Cadence, argued that Kaul's contention is totally false. "PKS is the only true integration of synthesis and place and route," he said. "Synopsys has no place and route technology to integrate and as a result suffers poor correlation, resulting in iteration."

Based on commentary in ESNUG and on a Matrox presentation, Estrada said Synopsys' beta customers are still describing multiple iterations in closing timing. "PKS users are experiencing single-pass timing closure," he said. " Stay tuned for announcements on this front."

Physical Compiler is available in limited release now; full production release is set for April 2000. Synopsys promises additional relationships with semiconductor vendors and customers by the end of 1999.

LOAD-DATE: November 13, 1999

8 of 15 DOCUMENTS

Electronic Engineering Times

February 7, 2000

SECTION: Times People, Pg. 131, INDUSTRY GADFLY

LENGTH: 486 words

HEADLINE: What the 'bug talk' tells us

BYLINE: JOHN COOLEY

BODY:

If you want to know how the five-way physical-synthesis horse race is going, you've got to track what the engineers who actually use such tools are saying and, more important, the bugs they find. (You can find such talk in newsgroups, on ESNUG or wherever engineers hang out.) Everything else is fluff designed to woo Wall Street and the more gullible EDA buyers.

Engineers who actually use a tool will have some praise and lots of gripes. It's human nature. No software is bug-free. When you're seeing lots of public bug talk about a tool, you truly know that it's being widely used. When you see only public smiles and sunshine about a tool, be aware that you're the one being used.

Having said this, here's the status of the RTL-to-GDS-II race as of early February. With the exception of Synopsys and Monterey, most of the EDA vendors (Cadence, Avanti and Magma) seem stuck in taxicab mode with their physical-synthesis tools. Taxicab mode is where the EDA vendor provides both the software and its own engineers, to drive the software at the customer site. It means the software is too unstable for real customer use.

Most of the 70 big-money EDA customers are buying only evaluation copies and holding private taxicab races-which is why I laughed when newbie Cadence CEO Ray Bingham bragged in a Jan. 25 press release about the company's PKS having 11 new "customers." Bingham's hotel-finance background, and his lack of any engineering experience, shows here.

The big breakthrough happened three months ago, when a real chip designer, Bob Prevett of Nvidia, wrote a detailed technical review in ESNUG 335 of PhysOpt (now called Physical Compiler) from Synopsys. A week later, Matrox and Nvidia both announced they had done chip tape-outs with Physical Compiler.

Then another real chip designer, Jon Stahl of Avici, wrote a detailed technical review of Synopsys' Chip Architect in ESNUG 338. That meant Synopsys was clearly moving out of taxicab mode.

Cadence PKS was believed to be struggling with three conflicting timing engines among PKS, Qplace and Pearl. Then, in SNUG 342, Jay McDougal of Agilent reported only a 0 to 3 percent timing error among PKS, Qplace, Pearl and even PrimeTime. (McDougal's short comment is the first known actual- customer usage statement about PKS.)

Avanti and a very noisy Magma are playing up vague customer endorsements , but nothing verifiable, in the press. Monterey's just a town in California. These are still taxicab companies. So, with two customer tapeouts vs. a first customer mention, it appears that Synopsys is about six months ahead of Cadence in physical synthesis. Watch the bug talk to see whether Synopsys stays ahead or falls behind.

JOHN COOLEY RUNS THE E-MAIL SYNOPSYS USERS GROUP (ESNUG), IS A CONTRACT ASIC DESIGNER AND LOVES HEARING FROM ENGINEERS AT JCOOLEY@WORLD.STD.COM OR (508) 429-4357.

LOAD-DATE: February 5, 2000

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Electronic Engineering Times

March 27, 2000

SECTION: Design Automation, Pg. 80, TOOL TALK

LENGTH: 417 words

HEADLINE: Show us the silicon

BYLINE: RICHARD GOERING

BODY:

In recent months we've heard about a number of EDA products that promise to revolutionize the way large chips are designed. But something is missing from most of these announcements: real customers who have taped out working chips using production-ready versions of the software.

Certainly, the announcements sound exciting. They include "physical synthesis" products from Synopsys and Cadence Design Systems; complete physical design systems from Monterey Design Systems and Magma Design Automation; and optimization and placement tools from Sapphire Design Automation and Silicon Perspective. This week alone, Cadence will add to its physical synthesis portfolio, and Synplicity is claiming to have the first physical synthesis for FPGAs.

The announcements are always accompanied by bold claims. The new tools, we're told, provide performance gains of 10, 20 or 50 percent; shave die size by 10 or 20 percent; and slash design cycles from months to days. Sometimes there are testimonials from "development partners" citing huge gains, usually based on limited test cases rather than actual working silicon.

But promising as they may be, the new products aren't real until someone designs and sells chips. Until then, they're in what John Cooley calls " taxicab mode," which is when vendors drive preproduction software and support engineers over to the customer's site and run the tools themselves.

Synopsys raised the bar with its Physical Compiler announcement last November. Up on stage were two users-Bogdan Staicu from Matrox Electronic Systems and Chris Malachowsky of Nvidia-who had actually taped out chips using Physical Compiler. Even though they had only used the tool's gate-level capabilities, they were able to cite some very specific metrics about performance gains and time savings, and to participate in an uncensored question-and-answer session.

That brings me to what we might call the EE Times Tapeout Challenge. For high-profile chip design products introduced within the past year, give us the name of a real user who has taped out an actual, commercial chip with the tool and who can speak on the record about his or her experience. Several such stories could turn into an interesting article.

And to EDA user companies, we say: Let your engineers speak. There must be a free flow of information for this industry to move forward, and we need a strong user voice in publications like EE Times.

http://www.eetimes.com/

LOAD-DATE: March 25, 2000

FOCUS - 10 of 56 DOCUMENTS

Business Wire

May 17, 2000, Wednesday

DISTRIBUTION: Business Editors

LENGTH: 787 words

HEADLINE: Synopsys' Physical Compiler Becomes Widely Available to Electronics Design Community

DATELINE: MOUNTAIN VIEW, Calif., May 17, 2000

BODY:

Leadership Position Established with Eight Communications and Graphics Tape-outs using Synopsys' Physical Compiler

Synopsys, Inc. (Nasdaq:SNPS) will make Physical Compiler, its unified synthesis and placement product, widely available to electronics designers starting May 22. The product, which was announced last November, was initially made available to only a limited number of customers. With eight tape-outs in the last six months, Physical Compiler has proven to be successful on a variety of high-performance design applications including graphics, third-generation (3G) wireless, satellite, and telecommunications.

"Synopsys has always been careful to ensure that our products are meeting or exceeding expectations before making them widely available to the design community," said Sanjiv Kaul, vice president and general manager for Synopsys' Physical Synthesis business unit. We also wanted to have experienced technical support in place. With the rate of tape-out successes we have seen, and having trained more than 100 engineers to support the product, it's time to make the product more widely available to all customers. "We're well-positioned to support new Physical Compiler customers and are pleased to see repeat purchases from existing customers that have each achieved successful tape-outs."

Customers Reach Quick Timing Closure and Tape-out Using Physical Compiler

Customers who have reached rapid timing closure and successful tape-out using Physical Compiler include Matrox Electronic Systems Ltd., NVIDIA Corporation, STMicroelectronics and Texas Instruments. In all cases, these companies have achieved timing closure in a matter of days versus weeks or months. ASIC vendors who have already announced design kit availability dates for Physical Compiler include IBM, NEC and STMicroelectronics.

"The tremendous productivity and performance gains that our customers have seen with Physical Compiler have resulted in several multi-million dollar repeat orders," said Sandeep Khanna, senior director of marketing for Synopsys' Physical Synthesis business unit. "Synopsys is working with more than 60 companies to integrate Physical Compiler into their existing design flows. These include the 4 or 5 top market leaders in communications, computing, graphics, and wireless, who have an immediate need to deploy Physical Compiler." Since many of these companies are working on complex designs, the widespread availability of Physical Compiler will make it easier for them to have access to the performance tools they need to help them achieve faster timing closure and meet time-to-market demands.

Synopsys' Physical Synthesis Solution

Pioneered by Synopsys, Physical Synthesis helps designers address the implementation challenges of next-generation ASIC and system-on-chip designs. Physical Synthesis brings key physical design considerations to the front-end, allowing RTL designers to achieve high quality area, timing and power quickly. The overall design flow includes Chip Architect design planner, Physical Compiler unified synthesis and placement tool and FlexRoute top-level router. It leverages industry-standard tools like Design Compiler(TM), Module Compiler(TM) and PrimeTime(R). Its proven interfaces to third-party solutions allow it to easily plug into an existing design flow.

Synopsys will showcase products designed with Physical Synthesis at the Design Automation Conference in Los Angeles (Booth 4201), June 5-8, 2000.

Pricing and Availability

Physical Compiler is available starting May 22. Pricing for a single-user, one-year term license begins at **$100,000. Support and maintenance options vary and are in addition to the product license.**

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS), headquartered in Mountain View, California, creates leading electronic design automation (EDA) tools for the global electronics market. The company delivers advanced design technologies and solutions to developers of complex integrated circuits, electronic systems, and systems on a chip. Synopsys also provides consulting and support services to simplify the overall IC design process and accelerate time to market for its customers. Visit Synopsys at http://www.synopsys.com.

Note to Editors: Synopsys and PrimeTime are registered trademarks of Synopsys, Inc., Design Compiler and Module Compiler are trademarks of Synopsys, Inc. All other trademarks or registered trademarks mentioned in this release are the intellectual property of their respective owners.

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sonia_harrison@kvo.com

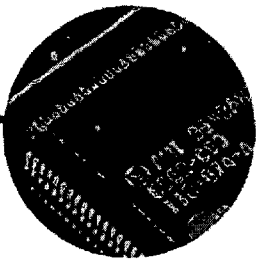
URL: http://www.businesswire.com

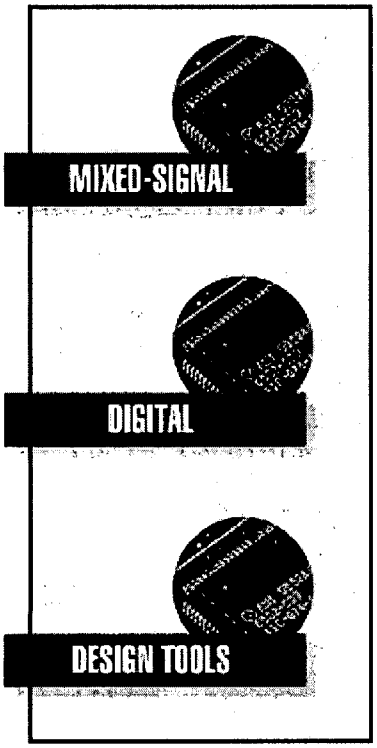
LOAD-DATE: May 18, 2000

EXHIBIT 77

AMI
AMERICAN MICROSYSTEMS, INC

Custom ASICs





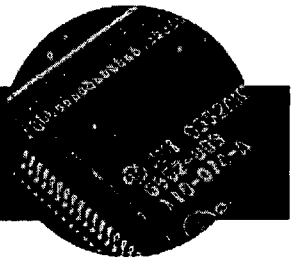
AMI literally pioneered the ASIC industry, introducing the first custom integrated circuits to the marketplace in 1966. Since then, the company has built on that experience to become an ASIC manufacturer with a worldwide reputation for low cost, high reliability, and flexibility in manufacturing processes.

Mixed-Signal | Digital | Design Tools

EXHIBIT 78

AMI
AMERICAN MICROSYSTEMS, INC.

Design Tools



AMI supports the ASIC design process with design kits for industry standard EDA tools and with its proprietary ACCESS Design Tools™.

AMI Design Kits

AMI Design Kits support EDA tools from vendors such as Synopsys, Viewlogic, Mentor, Cadence, Compass and Ikos. Design kits include cell libraries and software utilities to simplify the design process.

ACCESS Design Tools

ACCESS Design Tools put you in control of your ASIC development. AMI takes an industry leadership position in the development of expert system software for export to customer sites. The result is greatly shortened development spans, lower NRE, and increased first silicon success.

The ACCESS Design Tools are an integrated suite of software tools for digital ASIC verification, FPGA migrations, and fast prototyping through FPGAs. This proprietary software offering allows you to maintain complete control of an ASIC design or FPGA conversion in AMI's gate arrays and standard cell libraries.

NETRANS™

NETRANS services and software are the best in the industry for FPGA to ASIC migrations and ASIC second sourcing. NETRANS directly converts any FPGA or ASIC to an AMI gate array or standard cell circuit. Customers using FPGAs such as Xilinx, Altera and Actel can use the NETRANS software package in the ACCESS Design Tools to perform the conversion themselves.

NETRANSplus™

NETRANSplus allows you to achieve fast system prototyping by designing in AMI's gate array or standard cell libraries, then prototyping the system using FPGAs.

EXHIBIT 79

FOR IMMEDIATE RELEASE: November 28, 1995

CONTACT:

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Colorado Springs, CO 80907
719-594-8035 (voice)
719-594-8468 (fax)
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UTMC ANNOUNCES FULL VHDL TOOL KIT

COLORADO SPRINGS, CO -- UTMC Microelectronic Systems, Inc. (UTMC) today announced that one of the industry's first full VHDL (VHSIC Hardware Description Language) Design Kits will be available in the first quarter of 1996.

"Our VHDL Design Kit will really simplify high-level programming for our customers," said Greg Haynes, senior principal CAD engineer at UTMC. "ASIC designers have been eagerly awaiting VHDL tool kits, and we're delivering."

The UTMC Design Kit will allow customers to design across all VHDL simulators, including design, simulation (back-annotation, post lay-out delay information and accelerated gate-level simulations) and the creation of test programs. The Design Kit will be compatible with all VITAL compliant systems.

"Since VHDL was initially defined by the Department of Defense, and as the IEEE looks to endorse VITAL (VHDL Initiative Toward ASIC Libraries), VHDL has become very popular in military and commercial markets," said Haynes. "UTMC's VHDL Design Kit promises to enhance our customers' VHDL-based ASIC designs and systems."

UTMC, a manufacturer of semicustom and military-standard VLSI circuits, is dedicated to the aerospace and defense marketplace. UTMC has received Qualified Manufacturer List (QML) certification for Class V and Class Q. Additionally, UTMC has received a letter of compliance for ISO 9001 from the Defense Electronics Supply Center.

For product information call 1-800-MIL-UTMC, ext. 301, or write UTMC c/o LMS, 1036 Elkton Dr., Colorado Springs, CO 80907.

EXHIBIT 80

The SVP catalog provides an in-depth overview of each of our ASIC and FPGA partners. Each partner description includes a high-level design flow and methodology along with a detailed description of their technologies and the advantages of different architectures.

For a more detailed and searchable list of vendor's support of Synopsys libraries, check out the Library Listing Locator.

Introduction

Acronym Listing

SVP Locator

To request a copy of the complete SVP catalog, please send email to designinfo@synopsys.com

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Home Find Help FEEDBACK

EXHIBIT 81

SVP Library Locator

Select Vendor(s) ***(default=all)***

AMI
Actel
Advanced Micro Devices
Alcatel Mietec
Altera
Atmel

Locate | How To

Select Tool(s)

- ☐ Synthesis
- ☐ VSS
  - ☐ Vital
  - ☐ VSS Sign-off
- ☐ Test Synthesis
- ☐ Power Analysis
- ☐ DesignWare
- ☐ SmartModel Library

Select Geometries

1.0

Select Types(s)

- ☐ CBA
- ☐ FPGA
- ☐ Gate Array
- ☐ Standard Cell
- ☐ Embedded Array

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EXHIBIT 82

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Attorneys for Plaintiff Ricoh Company, Ltd.

UNITED STATES DISTRICT COURT
NORTHERN DISTRICT OF CALIFORNIA
SAN FRANCISCO DIVISION

RICOH COMPANY, LTD., Plaintiff, vs. AEROFLEX INC., AMI SEMICONDUCTOR, INC., MATROX ELECTRONIC SYSTEMS, LTD., MATROX GRAPHICS, INC., MATROX INTERNATIONAL, INC., MATROX TECH, INC., and AEROFLEX COLORADO SPRINGS, INC. Defendants.	Case No. C03-04669 MJJ (EMC) **AMENDED COMPLAINT**

Plaintiff Ricoh Company, Ltd. ("Ricoh") for its Complaint against Defendants Aeroflex Incorporated ("Aeroflex"), AMI Semiconductor, Inc. ("AMI"), Matrox Electronic Systems Ltd. ("Matrox"), Matrox Graphics Inc. ("Matrox Graphics"), Matrox International Corp. ("Matrox Int'l"), Matrox Tech, Inc. ("Matrox Tech"), and Aeroflex Colorado Springs, Inc. ("UTMC"), alleges as follows:

PARTIES

1. Plaintiff Ricoh is a corporation organized under the laws of Japan and maintains its principal place of business at 3-6 1-chome, Nakamagome, Tokyo, Japan.

2. Upon information and belief, Defendant Aeroflex is a corporation organized under the laws of the State of Delaware, and maintains its principal place of business at 35 S. Service Road, Plainview, NY, 11803. Aeroflex is doing business in this jurisdiction and/or has committed the acts complained of in this jurisdiction, and has consented to the jurisdiction of this Court for this action.

3. Upon information and belief, Defendant AMI is a corporation organized under the laws of the State of Delaware, and maintains its principal place of business at 2300 Buckskin Road, Pocatello, ID 83201. AMI is doing business in this jurisdiction and/or has committed the acts complained of in this jurisdiction, and has consented to the jurisdiction of this Court for this action.

4. Upon information and belief, Defendant Matrox is a corporation organized under the laws of Quebec, Canada, maintains its principal place of business at 1055 Boul St-Regis, Dorval, Quebec H9P 2T4 Canada. Matrox is doing business in this jurisdiction and/or has

committed the acts complained of in this jurisdiction, and has consented to the jurisdiction of this Court for this action.

5. Upon information and belief, Defendant Matrox Graphics is a corporation organized under the laws of Quebec, Canada, maintains its principal place of business at 1055 Boul St-Regis, Dorval, Quebec H9P 2T4 Canada. Matrox Graphics is doing business in this jurisdiction and/or has committed the acts complained of in this jurisdiction, and has consented to the jurisdiction of this Court for this action.

6. Upon information and belief, Defendant Matrox Int'l is a corporation organized under the laws of New York, maintains its principal place of business at 625 State Rt 3, Unit B, Plattsburgh, NY 12901. Matrox Int'l is doing business in this jurisdiction and/or has committed the acts complained of in this jurisdiction, and has consented to the jurisdiction of this Court for this action.

7. Upon information and belief, Defendant Matrox Tech is a corporation organized under the laws of the State of Delaware, maintains its principal place of business at 1075 Broken Sound Parkway, NW, Boca Raton, FL 33487-3524. Matrox Tech is doing business in this jurisdiction and/or has committed the acts complained of in this jurisdiction, and has consented to the jurisdiction of this Court for this action.

8. Upon information and belief, Defendant UTMC is a wholly-owned subsidiary of Defendant Aeroflex, is also known as Aeroflex Microelectronic Solutions, Inc., Aeroflex UTMC Microelectronic Solutions, Inc., and formerly known as United Technologies Microelectronics Center, is a corporation organized under the laws of the State of Delaware

and maintains a place of business at 4350 Centennial Blvd, CO, 80907. UTMC is doing business in this jurisdiction and/or has committed the acts complained of in this jurisdiction, and has consented to the jurisdiction of this Court for this action.

JURISDICTION

9. This action arises under the patent laws of the United States, Title 35, United States Code, and more particularly under 35 U.S.C. §§ 271 et. seq.

10. This Court has subject matter jurisdiction over this patent infringement action under the Judicial Code of the United States, 28 U.S.C. §§ 1338(a) and 1331.

11. This Court has personal jurisdiction over the Defendants because Defendants are present and/or doing business in this jurisdiction either directly or through their agents, or alternatively, have consented to the jurisdiction of this Court.

VENUE

12. Venue is proper in this district pursuant to 28 U.S.C. § 1391 in that Defendants regularly transact business in this judicial district and/or a substantial part of the events or omissions giving rise to the claim occurred in this judicial district and/or are found in this judicial district and/or are aliens.

FACTUAL BACKGROUND

13. On May 1, 1990, the U.S. Patent and Trademark Office ("USPTO") duly and legally issued United States Letters Patent No. 4,922,432 (the " '432 Patent") in the names of Hideaki Kobayashi and Masahiro Shindo for their invention titled "Knowledge Based Method and

Apparatus for Designing Integrated Circuits using Functional Specifications." A copy of the '432 Patent is attached hereto as Exhibit 1.

14. By assignment, Ricoh is the owner of the entire right, title, and interest in the '432 Patent and has the sole right to sue and recover for infringement thereof.

15. The '432 Patent describes, inter alia, a method for designing an application specific integrated circuit. By using the invention of the '432 Patent, one can define functional architecture independent specifications for an integrated circuit and translate functional architecture independent specifications into the detailed information needed for directly producing the integrated circuit.

PATENT INFRINGEMENT

COUNT 1

16. Ricoh repeats and realleges the allegations set forth in paragraphs 1 through 15 hereof.

17. Upon information and belief, Aeroflex has been and is now infringing the '432 Patent by utilizing in the United States the process of one or more of claims 13-17 of the '432 Patent as part of the process of manufacturing application specific integrated circuits, and/or by selling, offering to sell and/or importing into the United States, application specific integrated circuits made with the use and/or by the process of one or more of claims 13-17 of the '432 Patent, either literally or under the doctrine of equivalents.

18. Upon information and belief, Aeroflex will continue to infringe the '432 Patent unless enjoined by this Court.

19. As a consequence of Aeroflex's infringement, Ricoh has been irreparably damaged to an extent not yet determined, and Ricoh will continue to be irreparably damaged by such acts in the future unless Aeroflex is enjoined by this Court from committing further acts of infringement.

20. Upon information and belief, Aeroflex's infringement of the '432 Patent is willful.

21. Ricoh is entitled to recover damages adequate to compensate for Aeroflex's infringement.

COUNT 2

22. Ricoh repeats and realleges the allegations set forth in paragraphs 1 through 15 hereof.

23. Upon information and belief, AMI has been and is now infringing the '432 Patent by utilizing in the United States the process of one or more of claims 13-17 of the '432 Patent as part of the process of manufacturing application specific integrated circuits, and/or by selling, offering to sell and/or importing into the United States, application specific integrated circuits made with the use and/or by the process of one or more of claims 13-17 of the '432 Patent, either literally or under the doctrine of equivalents.

24. Upon information and belief, AMI will continue to infringe the '432 Patent unless enjoined by this Court.

25. As a consequence of AMI's infringement, Ricoh has been irreparably damaged to an extent not yet determined, and Ricoh will continue to be irreparably damaged by such acts in the future unless AMI is enjoined by this Court from committing further acts of infringement.

26. Upon information and belief, AMI's infringement of the '432 Patent is willful.

27. Ricoh is entitled to recover damages adequate to compensate for AMI's infringement.

COUNT 3

28. Ricoh repeats and realleges the allegations set forth in paragraphs 1 through 15 hereof.

29. Upon information and belief, Matrox has been and is now infringing the '432 Patent by utilizing in the United States the process of one or more of claims 13-17 of the '432 Patent as part of the process of manufacturing application specific integrated circuits, and/or by selling, offering to sell and/or importing into the United States, application specific integrated circuits made with the use and/or by the process of one or more of claims 13-17 of the '432 Patent, either literally or under the doctrine of equivalents.

30. Upon information and belief, Matrox will continue to infringe the '432 Patent unless enjoined by this Court.

31. As a consequence of Matrox's infringement, Ricoh has been irreparably damaged to an extent not yet determined, and Ricoh will continue to be irreparably damaged by such acts in the future unless Matrox is enjoined by this Court from committing further acts of infringement.

32. Upon information and belief, Matrox's infringement of the '432 Patent is willful.

33. Ricoh is entitled to recover damages adequate to compensate for Matrox's infringement.

COUNT 4

34. Ricoh repeats and realleges the allegations set forth in paragraphs 1 through 15 hereof.

35. Upon information and belief, Matrox Graphics has been and is now infringing the '432 Patent by utilizing in the United States the process of one or more of claims 13-17 of the '432 Patent as part of the process of manufacturing application specific integrated circuits, and/or by selling, offering to sell and/or importing into the United States, application specific integrated circuits made with the use and/or by the process of one or more of claims 13-17 of the '432 Patent, either literally or under the doctrine of equivalents.

36. Upon information and belief, Matrox Graphics will continue to infringe the '432 Patent unless enjoined by this Court.

37. As a consequence of Matrox Graphics' infringement, Ricoh has been irreparably damaged to an extent not yet determined, and Ricoh will continue to be irreparably damaged by such acts in the future unless Matrox Graphics is enjoined by this Court from committing further acts of infringement.

38. Upon information and belief, Matrox Graphics' infringement of the '432 Patent is willful.

39. Ricoh is entitled to recover damages adequate to compensate for Matrox Graphics' infringement.

COUNT 5

40. Ricoh repeats and realleges the allegations set forth in paragraphs 1 through 15 hereof.

41. Upon information and belief, Matrox Int'l has been and is now infringing the '432 Patent by utilizing in the United States the process of one or more of claims 13-17 of the '432 Patent as part of the process of manufacturing application specific integrated circuits, and/or

by selling, offering to sell and/or importing into the United States, application specific integrated circuits made with the use and/or by the process of one or more of claims 13-17 of the '432 Patent, either literally or under the doctrine of equivalents.

42. Upon information and belief, Matrox Int'l will continue to infringe the '432 Patent unless enjoined by this Court.

43. As a consequence of Matrox Int'l's infringement, Ricoh has been irreparably damaged to an extent not yet determined, and Ricoh will continue to be irreparably damaged by such acts in the future unless Matrox Int'l is enjoined by this Court from committing further acts of infringement.

44. Upon information and belief, Matrox Int'l's infringement of the '432 Patent is willful.

45. Ricoh is entitled to recover damages adequate to compensate for Matrox Int'l's infringement.

COUNT 6

46. Ricoh repeats and realleges the allegations set forth in paragraphs 1 through 15 hereof.

47. Upon information and belief, Matrox Tech has been and is now infringing the '432 Patent by utilizing in the United States the process of one or more of claims 13-17 of the '432 Patent as part of the process of manufacturing application specific integrated circuits, and/or by selling, offering to sell and/or importing into the United States, application specific integrated circuits made with the use and/or by the process of one or more of claims 13-17 of the '432 Patent, either literally or under the doctrine of equivalents.

48. Upon information and belief, Matrox Tech will continue to infringe the '432 Patent unless enjoined by this Court.

49. As a consequence of Matrox Tech's infringement, Ricoh has been irreparably damaged to an extent not yet determined, and Ricoh will continue to be irreparably damaged by such acts in the future unless Matrox Tech is enjoined by this Court from committing further acts of infringement.

50. Upon information and belief, Matrox Tech's infringement of the '432 Patent is willful.

51. Ricoh is entitled to recover damages adequate to compensate for Matrox Tech's infringement.

COUNT 7

52. Ricoh repeats and realleges the allegations set forth in paragraphs 1 through 15 hereof.

53. Upon information and belief, UTMC has been and is now infringing the '432 Patent by utilizing in the United States the process of one or more of claims 13-17 of the '432 Patent as part of the process of manufacturing application specific integrated circuits, and/or by selling, offering to sell and/or importing into the United States, application specific integrated circuits made with the use and/or by the process of one or more of claims 13-17 of the '432 Patent, either literally or under the doctrine of equivalents.

54. Upon information and belief, UTMC will continue to infringe the '432 Patent unless enjoined by this Court.

55. As a consequence of UTMC's infringement, Ricoh has been irreparably damaged to an extent not yet determined, and Ricoh will continue to be irreparably damaged by such acts in

the future unless UTMC is enjoined by this Court from committing further acts of infringement.

56. Upon information and belief, UTMC's infringement of the '432 Patent is willful.

57. Ricoh is entitled to recover damages adequate to compensate for UTMC's infringement.

PRAYER FOR RELIEF

WHEREFORE, Ricoh prays for entry of judgment:

A. that Aeroflex has infringed the '432 Patent;

B. that Aeroflex, its agents, employees, representatives, successors, and assigns and those acting, or purporting to act, in privity or in concert with Aeroflex, be preliminarily and permanently enjoined from further infringement of the '432 Patent;

C. that Aeroflex account for and pay to Ricoh all damages under 35 U.S.C. § 284, including enhanced damages, caused by the infringement of the '432 Patent, and attorneys' fees pursuant to 35 U.S.C. § 285;

D. that Ricoh be granted pre-judgment and post-judgment interest on the damages caused to it by reason of Aeroflex's infringement of the '432 Patent;

E. that AMI has infringed the '432 Patent;

F. that AMI, its agents, employees, representatives, successors, and assigns and those acting, or purporting to act, in privity or in concert with AMI, be preliminarily and permanently enjoined from further infringement of the '432 Patent;

G. that AMI account for and pay to Ricoh all damages under 35 U.S.C. § 284, including enhanced damages, caused by the infringement of the '432 Patent, and attorneys' fees pursuant to 35 U.S.C. § 285;

H. that Ricoh be granted pre-judgment and post-judgment interest on the damages caused to it by reason of AMI's infringement of the '432 Patent;

I. that Matrox has infringed the '432 Patent;

J. that Matrox, its agents, employees, representatives, successors, and assigns and those acting, or purporting to act, in privity or in concert with Matrox, be preliminarily and permanently enjoined from further infringement of the '432 Patent;

K. that Matrox account for and pay to Ricoh all damages under 35 U.S.C. § 284, including enhanced damages, caused by the infringement of the '432 Patent, and attorneys' fees pursuant to 35 U.S.C. § 285;

L. that Ricoh be granted pre-judgment and post-judgment interest on the damages caused to it by reason of Matrox's infringement of the '432 Patent;

M. that Matrox Graphics has infringed the '432 Patent;

N. that Matrox Graphics, its agents, employees, representatives, successors, and assigns and those acting, or purporting to act, in privity or in concert with Matrox Graphics, be preliminarily and permanently enjoined from further infringement of the '432 Patent;

O. that Matrox Graphics account for and pay to Ricoh all damages under 35 U.S.C. § 284, including enhanced damages, caused by the infringement of the '432 Patent, and attorneys' fees pursuant to 35 U.S.C. § 285;

P. that Ricoh be granted pre-judgment and post-judgment interest on the damages caused to it by reason of Matrox Graphics' infringement of the '432 Patent;

Q. that Matrox Int'l has infringed the '432 Patent;

R. that Matrox Int'l, its agents, employees, representatives, successors, and assigns and those acting, or purporting to act, in privity or in concert with Matrox Int'l, be preliminarily and permanently enjoined from further infringement of the '432 Patent;

S. that Matrox Int'l account for and pay to Ricoh all damages under 35 U.S.C. § 284, including enhanced damages, caused by the infringement of the '432 Patent, and attorneys' fees pursuant to 35 U.S.C. § 285;

T. that Ricoh be granted pre-judgment and post-judgment interest on the damages caused to it by reason of Matrox Int'l's infringement of the '432 Patent;

U. that Matrox Tech has infringed the '432 Patent;

V. that Matrox Tech, its agents, employees, representatives, successors, and assigns and those acting, or purporting to act, in privity or in concert with Matrox Tech, be preliminarily and permanently enjoined from further infringement of the '432 Patent;

W. that Matrox Tech account for and pay to Ricoh all damages under 35 U.S.C. § 284, including enhanced damages, caused by the infringement of the '432 Patent, and attorneys' fees pursuant to 35 U.S.C. § 285;

X. that Ricoh be granted pre-judgment and post-judgment interest on the damages caused to it by reason of Matrox Tech's infringement of the '432 Patent;

Y. that costs be awarded to Ricoh; and

Z. that Ricoh be granted such other and further relief as the Court may deem just and proper under the current circumstances;

AA. that UTMC has infringed the '432 Patent;

BB. that UTMC, its agents, employees, representatives, successors, and assigns and those acting, or purporting to act, in privity or in concert with UTMC, be preliminarily and permanently enjoined from further infringement of the '432 Patent;

CC. that UTMC account for and pay to Ricoh all damages under 35 U.S.C. § 284, including enhanced damages, caused by the infringement of the '432 Patent, and attorneys' fees pursuant to 35 U.S.C. § 285; and

DD. that Ricoh be granted pre-judgment and post-judgment interest on the damages caused to it by reason of UTMC's infringement of the '432 Patent.

Ricoh Company, Ltd.
By: _____/s/_____
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